# A microprocessor-based, 9600 bit/s modem

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**Summary** Data transmission at 9600 bit/s over telephone circuits demands complex signal-processing techniques. A modem has been designed in which these processes are performed by a bit-slice microprocessor. Operating in a time-shared mode it performs the functions of modulation, demodulation, filtering, equalization, timing and phase recovery.

A single chip microcomputer controls data, interfaces and self-test loops to the four multiplexed data ports.

The modem comprises three printed-circuit boards, a power unit and an optional public service telephone network interface unit.

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Since 1980 he has represented the Company on CCITT Study Group XVII which is concerned with data transmission over the telephone network.

## Introduction

The ability to transmit data at 9600 bit/s over a telephone circuit offers real advantages to the user of data communication systems. For real-time systems, such as computer-aided design (c.a.d), it speeds the response of the computer to the remote terminal; for batch-mode operation it allows the multiplexing of a number of low-speed data channels with a subsequent saving in line costs.

Analogue telephone circuits, with their limited bandwidth and inherent amplitude and phase distortions, demand the use of special signal-processing techniques in data modems operating at higher speeds. As integrated circuit and microprocessor technology has advanced, so it has become possible to implement these techniques in a compact unit.

To illustrate this point, a data modem will be described that has been designed to transmit data at 9600, 7200 or 4800 bit/s over leased circuits, and which can be adapted to operate over public networks. New signal-processing techniques to enhance the public network operation will also be described briefly.

## Transmission characteristics

The characteristics of a 9600 bit/s modem to operate on leased telephone circuits are standardized in CCITT Recommendation V29.[1] This recognizes the constraints imposed by the circuits and embodies techniques to overcome them.

### Signalling rate

The group delay and attenuation slope at the band edges of a telephone channel limit signalling rates to between 2500 and 3000 bauds. Data at higher rates must be encoded into multi-bit symbols before transmission. At 9600 bit/s the data are encoded into 4-bit symbols and transmitted at 2400 bauds.

The 16 possible signal conditions are

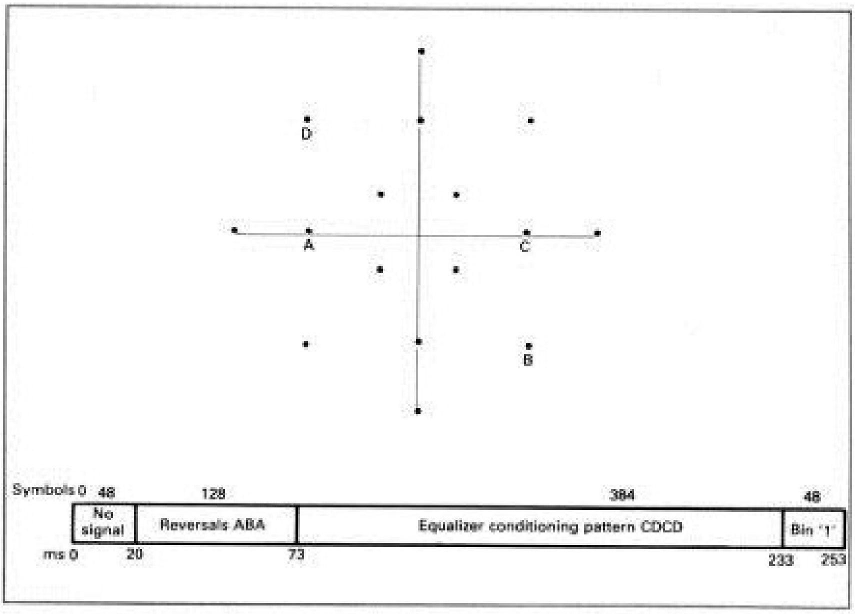



*Fig. 1. V29 Space pattern and initializing sequence.*

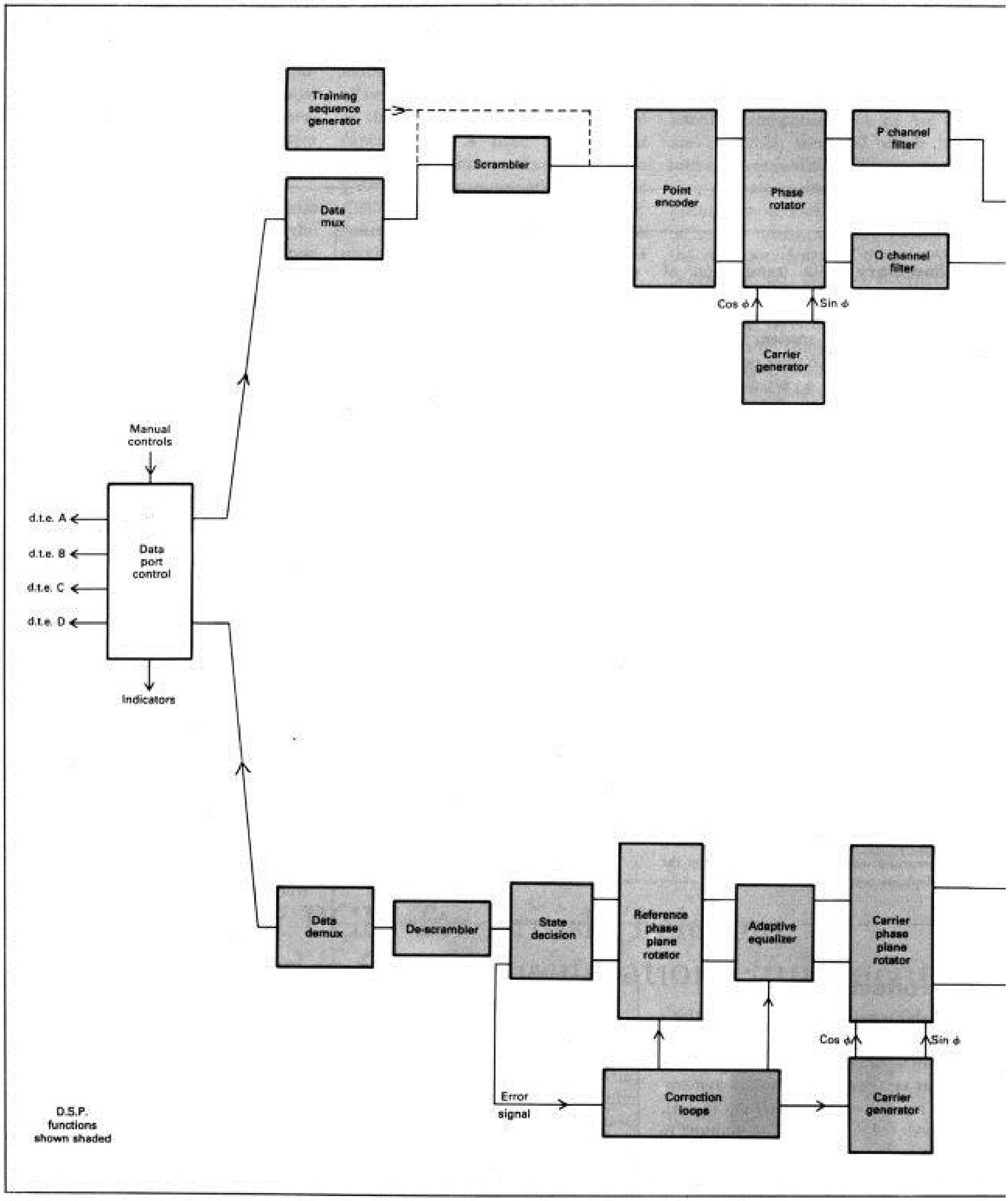



*Fig. 2. Marconi 9600 Modem functional block diagram.*

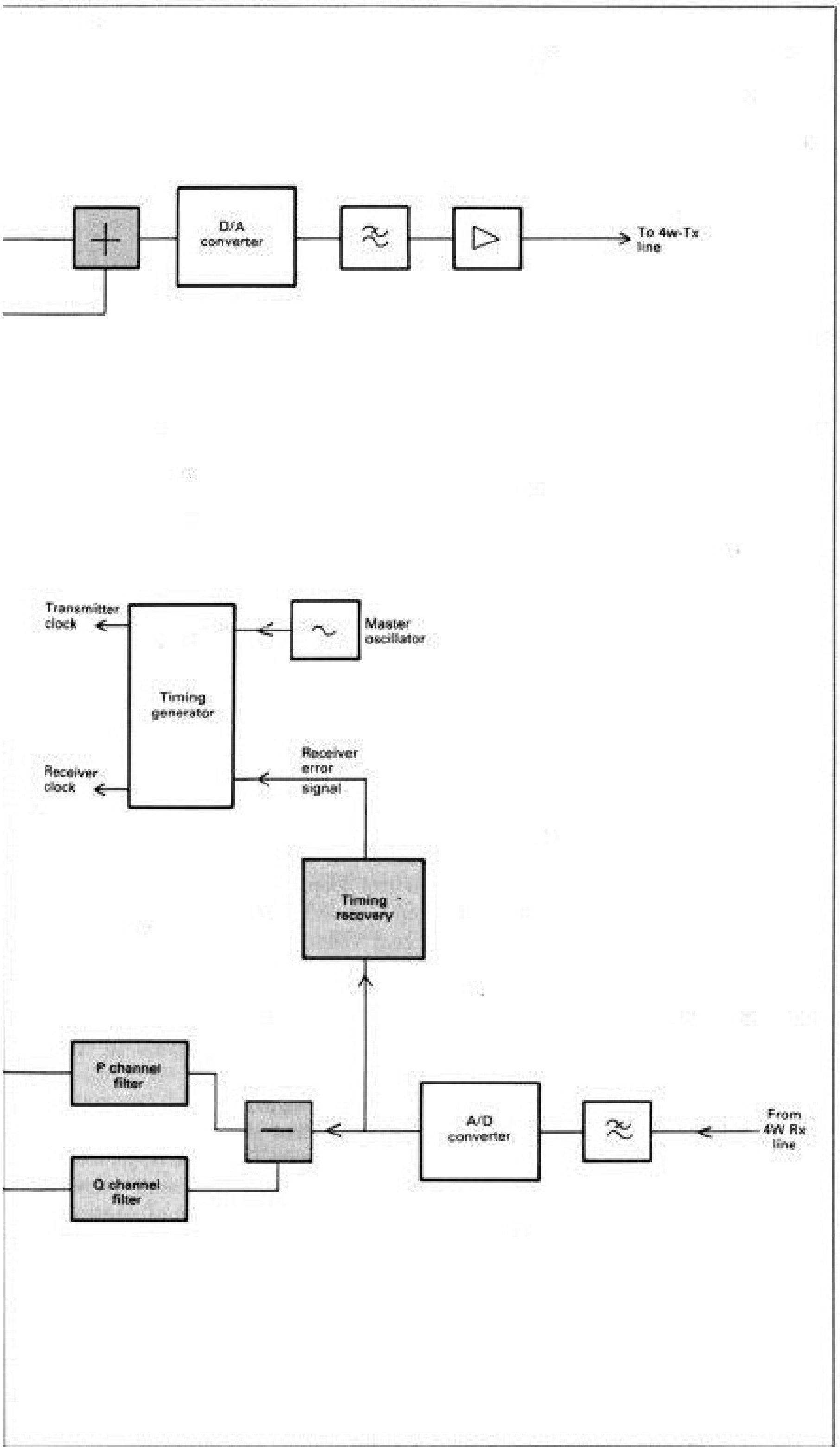
formed into a space pattern representing discrete phase/amplitude vectors of a 1700 Hz carrier (figure 1). Use of Gray encoding ensures that adjacent coding points differ from each other by only one or, at most, two bits.

Recognizing that line conditions may not always permit transmission at the maximum rate, provision is made to fall back to speeds of 7200 or 4800 bit/s. The modulation rate remains at 2400 bauds but the space pattern is reduced to eight phase points with 3-bit symbols at 7200 bit/s, and four phase points with 2-bit symbols at 4800 bit/s.

**Training sequence**

Because of the distortion to the signal which is introduced by the channel, it is necessary for a standardized preamble to be sent on which the receiver may train its adaptive circuits.

The sequence laid down in V29 comprises three periods. First, 128 AB




alternations (figure 1) are sent to allow the receiver to acquire carrier frequency, carrier phase and symbol timing. Next follows a sequence of CD alternations which the adaptive equalizer uses to set its tap coefficients to the values needed to correct for the time dispersions of the channel. Finally, 48 scrambled binary ones are sent. Scrambling completely randomizes the data and so all 16 symbol combinations may be sent, enabling the receiver to optimize its synchronization and equalizer settings. During data transmission, the receiver is continually adapting these settings to changes in the received signal created by the channel. Should it 'lose' the signal, and errors become unacceptably high, it will automatically send a training sequence to the distant modem. The distant modem will respond with a training sequence. Exchange of sequences continues at intervals until satisfactory conditions are achieved again, or a pre-set time-out operates.

### Multiplexing

Within a modem, various combinations of 2400, 4800 and 7200 bit/s channels may be multiplexed together to form a 9600 bit/s aggregate data stream. V29 standardizes the alternative combinations and encoding for four data ports.

## The Marconi 9600 Modem

This modem has been designed to conform to the V29 characteristics described above. It differs from a modem employing discrete functional circuits in that all the signal-processing functions and the control functions are performed by microprocessors under stored program control.

A digital signal processor (d.s.p), comprising a 12-bit, high-speed, bipolar microprocessor, a multiplier/accumulator and associated memory banks, performs all the functions shown in the shaded portion of figure 2. While the diagram shows the sequence of functions in conventional block schematic form, it should be appreciated that, in reality, they are carried out in a priority sequence by the d.s.p.

The exchange of signals between the d.s.p and the four data terminal equipment (d.t.e) ports, the manual and pre-set controls, and the indicators is under the control of a single-chip microcomputer.

### Transmitter

If operating in a multiplexing mode, data from each d.t.e port are taken in the pre-set sequence to form an aggregate stream. This is then randomized by a scrambler having the generating polynomial $1 + X^{-18} + X^{-23}$. The data bits are then assembled into symbols from which the correct modulation point is encoded. Before data transmission, the V29 training sequence is generated and applied to the modulation point encoder.

The complex, 16-state signal is generated by modulating either an in-phase (P) or quadrature (Q) carrier by one of eight phase/amplitude levels. The

*Fig. 3. The Marconi Modem 9600.*

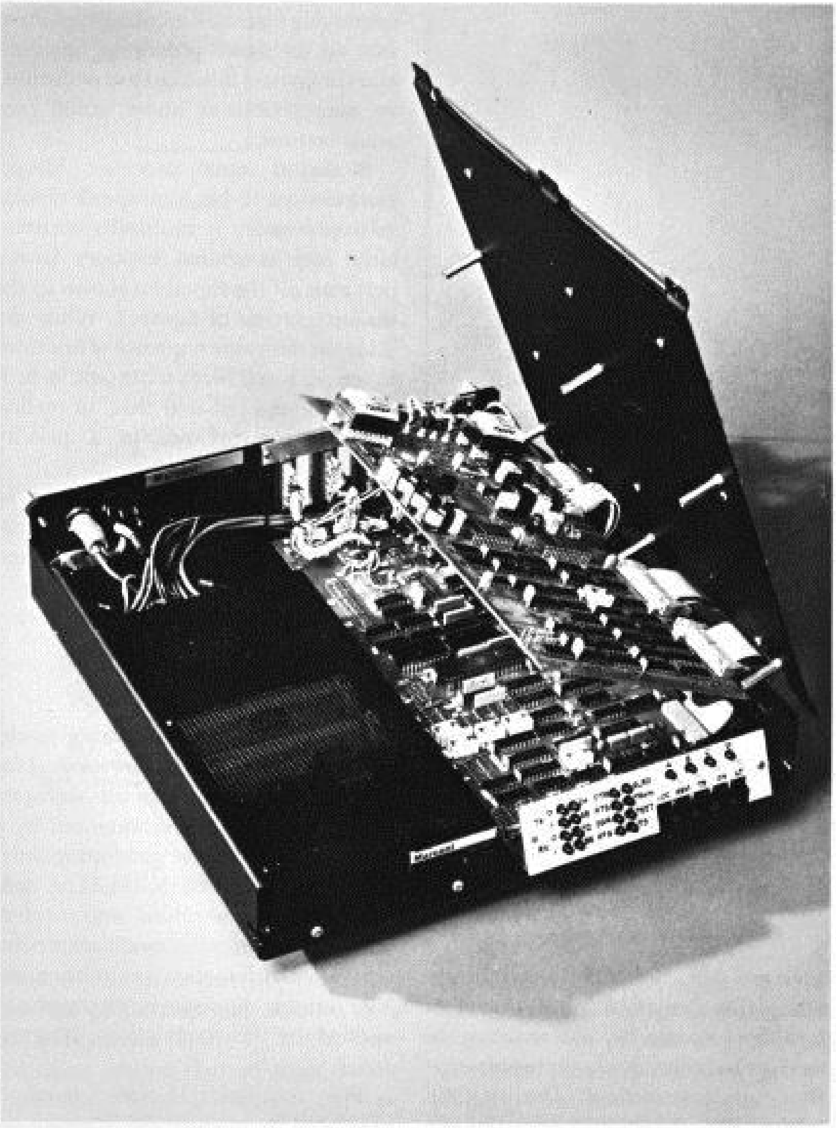


*Fig. 4. Marconi Modem 9600 – exploded view showing the analogue timing board and, below it, the control board and power supply unit.*

resultant P and Q channels are digitally filtered before summing to produce the composite signal in digital form. A 12-bit digital-analogue converter forms the analogue signal which, after low-pass filtering, is transmitted to line.

### Receiver

Line signals are low-pass filtered, sampled at a rate of 9600 samples per second, then converted to 12-bit digital words and input to the d.s.p. Symbol timing is recovered at this point by examination of the band-edge components of the received signal. This information is used to synchronize the receive timing generator to the signal.

Demodulation is complementary to the modulation process. The P and Q channel signals are extracted by the 32-tap, finite impulse response (f.i.r) digital filters and the real and imaginary baseband components are extracted by the cos $\phi$ and sin $\phi$ local carriers.

The adaptive equalizer comprises a 32-tap, complex, f.i.r digital filter, the tap coefficients of which are adjusted automatically to compensate for the time dispersions of the channel. Initial adjustment is made by reference to the second sequence of the training pattern sent by the transmitter. The gain of the control loop is large initially but, as convergence is approached and the error signal reduces, the gain is reduced. During data transmission the gain is at minimum and only fine adjustments are made to the tap weightings to compensate for slow variations in the channel.

Equalized signals are compared with a reference phase plane to determine the correct value for the received symbols. The phase plane is rotated to the correct position during the training sequence and, like the equalizer, it is adaptively adjusted during transmission.

Error signals for the control loops are derived from the state decision function and are based on the scatter of signals from their reference points.

The decoded signal is descrambled and the data routed to their correct data ports in accordance with the multiplexing configuration selected.

### D.T.E interfaces

Four data ports are each served by a set of interface circuits in accordance with CCITT Recommendations V24[2] and V29. When operating in a multiplex mode it is necessary that all d.t.es share a common clock derived from the modem, a selected port, or the received data. Otherwise the four ports are inde-

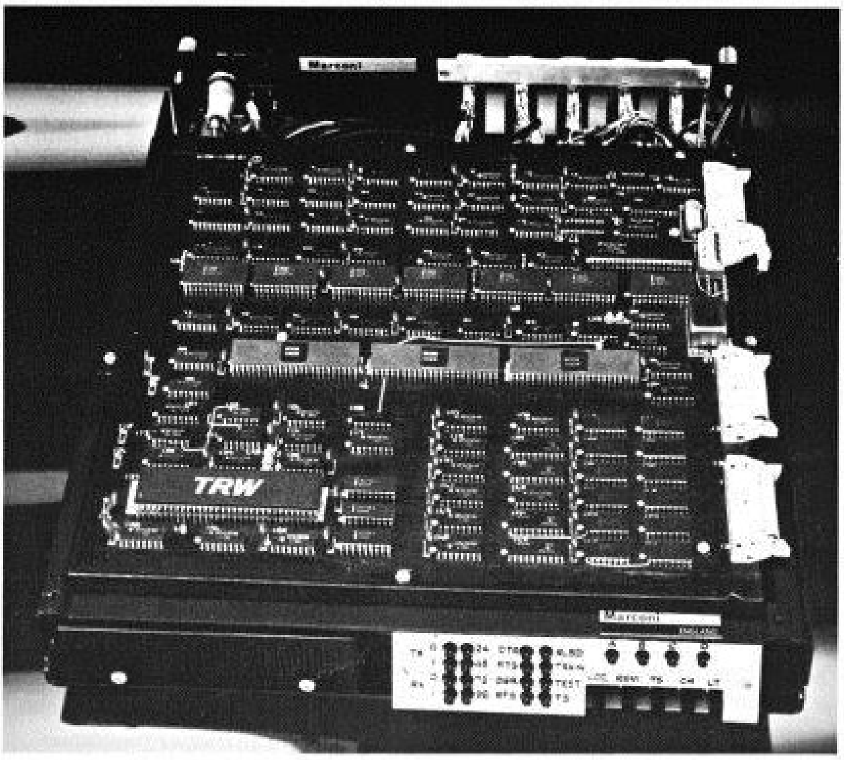



*Fig. 5. Marconi 9600 Modem – top view showing the d.s.p board.*

pendent of each other. Switched-carrier operation can be simulated on each channel by signalling the OFF condition of Circuit 105 (Request to Send) at the transmitting port to the distant receiver. On detection of this signal, Circuit 109 (Line Signal Detector) is turned OFF at the receiving port.

### Test looping

In the event of a system failure it is important that the fault be isolated quickly. The four test loops defined in CCITT Recommendation V54[3] provide for this by looping the signal back at the local d.t.e interface, the local line-interface, the remote line-interface or the remote d.t.e interface. Intelligent use of these loops can progressively isolate a fault in either modem or the channel. The modem provides for both analogue and digital test loops to be established, and a test pattern to be transmitted and checked.

In the local analogue loop condition the modem is disconnected from line and the transmit signal linked to the receiver input. A complete local test of the modem can then be made by the use of an internally generated test pattern which can be error checked. This loop condition can be established manually by push-switch, or electrically by Circuit 141 on Channel A.

A digital test loop on any channel can be set up with a remote modem conforming to the latest revision of CCITT Recommendation V54. The loop is instigated by the local modem transmitting a unique data pattern on the channel it is desired to loop back. The remote modem, on recognition of this pattern, will connect Received Data (Circuit 104) to Transmitted Data (Circuit 103), at the same time isolating those circuits from the d.t.e. The Test Indicator (Circuit 142) is turned ON. The test pattern may then be sent by the local modem and, after the round trip, checked for errors. Termination of the loop condition is made by the transmission of a longer discrete pattern, on the recognition of which the remote modem returns the channel under test to the normal condition and turns Circuit 142 off. While the test is in progress the remaining data channels may operate normally.

### Implementation

The circuits comprising the modem are built on three printed-circuit-board assemblies. One contains the digital signal processor, one the timing and analogue components and the third the control processor.

### Digital signal processor

A 12-bit, bi-polar, bit-slice microprocessor, the AM 2903, with an external multiplier/accumulator, is employed to maximize the speed of computation. Working in a time-shared mode it is necessary to complete each convolution associated with the filtering and equalizing functions within 100 μs.

There are three areas of memory on the d.s.p: ROM, which stores the fixed-tap coefficients for the digital filters and the sine look-up table for the carrier generators; RAM, in which the equalizer-tap coefficients are held and continually updated as the channel varies; finally there is the program ROM, controlling the sequence of operations by the d.s.p.

The d.s.p is completely self-contained, requiring only external power and connections to its data highways. It can, as a result, be employed as a signal processor in a variety of applications.

### Analogue and timing circuits

Conversion between the 12-bit digital words and the analogue signals is carried out on this board which also contains the external analogue filters, buffer amplifiers and line-isolating transformers.

A master crystal oscillator and two divider chains provide the transmitter and receiver clock signals. Error signals from the timing recovery circuits bring the receiver clock into synchronism by momentarily changing the divide ratios.

### Control circuits

Control of the interface circuits to the four data ports, setting up of test loops, and interfacing to selection switches and indicators are carried out by the single chip 8049 microcomputer, which is mounted on the control board. The variety of optional facilities and modes of operation available can be pre-set by dual-in-line switches mounted on the board. Front-panel switches and indicators are connected directly to this board.

### Power unit

In order to minimize dissipation within the case, a high-efficiency, open frame, switched-mains power supply unit is used. It supplies d.c power at +5V, +12V and −12V to the three functional boards.

### Case assembly

The three printed-circuit boards are mounted within a metal chassis and interconnected by ribbon cable. The d.s.p and the analogue/timing boards are mounted either side of a metal plate which serves as a heat sink. Hinging of this plate allows access to the lower control board and the dual-in-line facility switches.

An easily removable metal cover includes a sliding Perspex window through which the l.e.d indicators can be viewed and the control switches operated when entering a manual test mode.

### Operator facilities

Means are provided for an operator to diagnose a system fault quickly.

Two control switches at the front of the modem instigate the setting up of either a local analogue loop or a remote digital loop. A further switch initiates transmission of the 511-bit, pseudo-random test pattern around the selected loop.

L.E.D indicators adjacent to the switches monitor the condition of Circuits 103, 104, 105, 106, 107, 108 and 109 on the selected d.t.e interface. Four more l.e.ds indicate which channel is being monitored. Other indicators show when a channel is in a test mode, and when a test pattern has been correctly received.

The dual in-line switches on the control board select the signal timing source, the combination of data rates on the four ports, constant carrier or simulated switched carrier mode of operation, and public or leased-circuit operation.

### Public switched telephone network (p.s.t.n) operation

The modem described can work directly on leased circuits, but for p.s.t.n operation there need to be additional facilities. To permit full duplex operation it is necessary with the V29 system to have a four-wire circuit. On p.s.t.n this can be achieved only by a double dial-up system. This in turn demands line-terminating facilities for two p.s.t.n lines. A separate unit, designed to fit beneath the modem case, will contain these circuits together with a fixed-compromise equalizer in the receive path to compensate for the band-edge slope in amplitude and group delay found on most p.s.t.n connections. The unit will derive its power from the modem unit, being interconnected with it by a multi-way cable.

It is envisaged that future modems of this type will employ echo-cancelling techniques to permit full duplex operation over a two-wire circuit. Such techniques are an extension of the digital signal-processing techniques described above and require only standardizing to allow their widespread use.

## References


1. CCITT Yellow Book Vol. VIII, Data Communication over the telephone network, V29 (Geneva 1976, amended at Geneva 1980). ITU, Geneva.
2. CCITT Yellow Book Vol. VIII, Data Communication over the telephone network, V24 (Geneva 1964, amended at Mar del Plata 1968 and at Geneva 1972, 1976 and 1980). ITU, Geneva.
3. CCITT Yellow Book Vol. VIII, Data Communication over the telephone network, V54 (Geneva 1976, amended at Geneva 1980). ITU, Geneva.



**RÉSUMÉ**

La transmission de données à 9600 bits/seconde sur circuits téléphoniques exige la mise en oeuvre de techniques de traitement de signaux extrêmement complexes. Dans un modem de conception récente, ces processus sont exécutés par un microprocesseur en tranches. Ce dispositif, qui fonctionne en temps partagé, assure les fonctions de modulation, de démodulation, de filtrage, de synchronisation d'égalisation et de rétablissement en phase.

Un micro-ordinateur à puce unique commande les données, les interfaces et les boucles d'autocontrôle des quatre accès d'information multiplexés.

Le modem comporte trois plaques de circuits imprimés, un bloc d'alimentation et un bloc d'interface facultatif pour raccordement au réseau téléphonique public commuté.

**ZUSAMMENFASSUNG**

Zur Datenübertragung bei einer Geschwindigkeit von 9600 Bit/s über Telefonkanäle benötigt man komplizierte Signalaufbereitungen. Es wurde ein Modem konstruiert, in dem diese Aufbereitungsschritte durch ein Bitscheiben-Mikroprozessor ausgeführt werden. Dieser erstellt die Modulations-, Demodulations-, Filtrier-, Entzerrungstakt-und Phasenerholungsfunktionen aus.

Ein aus einem einzelnem Chip bestehender Mikrocomputer steuert den Datenfluss und stellt die Schnittstelle sowie Selbstprüfung zu den vier Multiplex-Datenanschlüssen dar.

Der Modem besteht aus 3 Leiterplatten einer Stromversorgung und einer wahlweisen Schnittstelle zum Anschluss an die öffentliche Telefonvermittlung.

**RESUMEN**

La transmisión de datos a 9600 bit/s sobre circuitos telefónicos requiere técnicas complejas en el proceso de señal. Se ha diseñado un módem en el cual se ejecutan estos procesos mediante un microprocesador de cortes de bitios. Funcionando en un modo de subdivisión de tiempo, ejecuta las funciones de modulación, desmodulación, filtración, temporización de compensación y recuperación de fase.

Un microcomputador de viruta único controla los datos, entrecaras y bucles autoverificados a las cuatro portillas de datos múltiples.

El módem comprende tres tableros de circuito impreso, una unidad de potencia y una unidad opcional de entrecaras para conectar a redes telefónicas públicas de conmutación.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