A hypergroup codec

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Summary The United Kingdom trunk telephone network currently relies heavily on analogue frequency division multiplex (f.d.m) equipment operating over coaxial cable and radio relay systems. While the eventual aim is to replace this with a digital system, the transition is unlikely to be complete for several years.

In the interim period a need exists for a relatively simple and efficient means of carrying signals from existing f.d.m equipment over a digital link.

This article describes an equipment designed to carry a 900-channel f.d.m hypergroup signal over a 140Mbit/s digital link. Consideration is given to the choice of system parameters, noise performance and implementation.

T. H. Pearce
After serving a student apprenticeship with Marconi Instruments, St. Albans, followed by post graduate study at the University of Southampton, Mr Pearce joined Marconi Research Laboratories in 1968. There he has worked on various aspects of communication signal processing, including techniques for analogue-to-digital conversion and high-speed digital systems. More recently he has been involved with a variety of communication system studies, including study work for the f.d.m supergroup codec, also described in this issue. He is currently leading the hypergroup codec design team.

M. J. Whittemore
Joined Marconi Research Laboratories at Great Baddow in 1970 after undertaking a graduate training course. Before transferring to the Communications Laboratory he spent a period working on digital signal processing systems for radar. Since then he has worked on a variety of communication projects and system studies, including the development of high-rate digital multiplex equipment. Recently he has been engaged on the study and development of spread-spectrum communication systems. Mr Whittemore developed the frequency translation units for the hypergroup codec.

H. J. Pipe
Since completing a graduate apprenticeship with The Marconi Company, joining Communications Research at Baddow in 1963, Harvey Pipe has accumulated wide experience on projects including high stability crystal oscillators, digital facsimile, a modulation and coding study for Aerosat and, more recently, studies on data link feasibility. In the hypergroup codec he has developed the multiplex, demultiplex and associated timing units.

Introduction

Despite the general trend towards the use of digital techniques in electronic systems, the trunk telephone network still remains essentially an analogue system using the technique of frequency division multiplex (f.d.m) to separate channels. While digital techniques have been used to some extent, in the form of 24- and 30-channel pulse code modulation (p.c.m) multiplex equipment, this has so far been restricted to use on local junction routes between exchanges.

In the UK this situation is about to change. Techniques for the multiplexing and transmission of digitized telephone signals and other data, at rates in excess of 100Mbit/s, have been researched in many laboratories over the past decade and are now about to be put into practice. In an extensive investment programme extending over the next decade, British Telecom plan to replace the entire f.d.m trunk network with a digital transmission system operating at rates up to 140Mbit/s and possibly higher.

During the transition to this purely digital network, a need exists for a relatively simple and efficient means of carrying signals from existing f.d.m equipment over the new digital links, both as a means of loading these links in the early stages when only a limited amount of digitally-generated traffic is available, and subsequently to maintain flexibility within the network until eventually all f.d.m equipment is phased out.

The purpose of this article is to describe the design of an equipment currently being developed for British Telecom, which will enable a 900-channel f.d.m hypergroup signal to be conveyed over a 140Mbit/s digital link and to be recovered at the far end in its original f.d.m form. Consideration is given to the choice of system parameters, noise performance and implementation.

System description

The equipment consists essentially of the p.c.m encoder-decoder combination shown in figure 1.

At the encoder (figure 1a), the analogue f.d.m signal is applied to an analogue-to-digital (a–d) converter via the necessary amplification and filtering. In the specific case of the 900-channel hypergroup signal it is also necessary to provide an initial stage of frequency translation to match the pass-band of the f.d.m signal to the chosen sampling frequency adopted in the a–d converter. The digital output from the converter is in parallel form, requiring a digital multiplex to generate a single serial data stream for transmission. The transmission code adopted is coded mark inversion (c.m.i).

At the decoder (figure 1b), the f.d.m signal is recovered by means of a complementary demultiplex followed by a digital-to-analogue (d–a) converter, suitable output filtering and a complementary stage of frequency translation to return the f.d.m signal to its original frequency band.

The codec may also be operated without the frequency translators, with a corresponding saving in cost and complexity and a small improvement in noise performance. The capacity is reduced to that of the 14-supergroup assembly (840 channels) covering the band 312–3780kHz. The more likely application, however, is for the full 15-supergroup capacity requiring the translators.

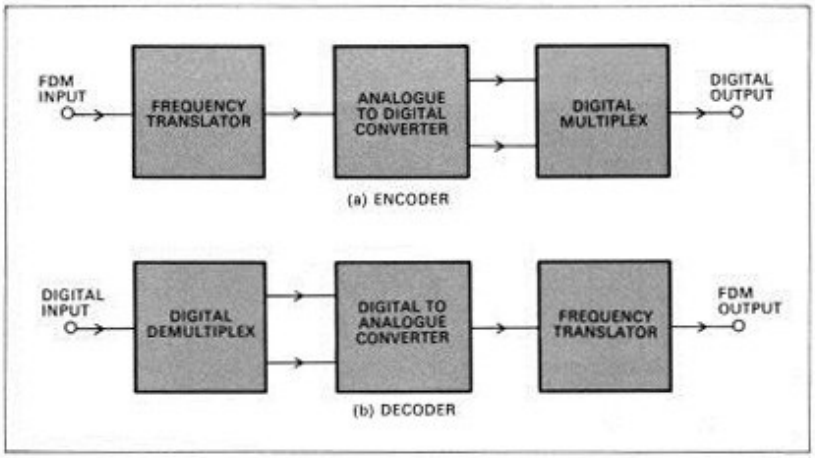

Fig. 1. Simplified block diagram of codec

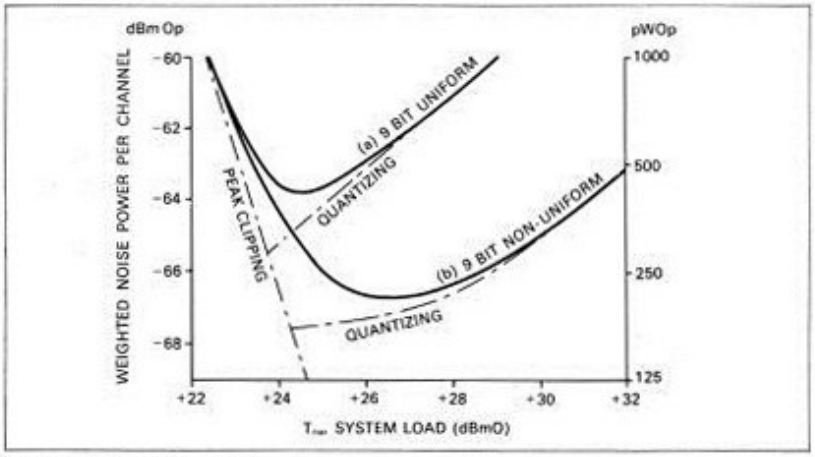

Fig. 2. Noise performance

System parameters

The system parameters, output bit rate, quantization accuracy and sampling frequency have been chosen to provide an efficient match between the bandwidth of the f.d.m signal and the bit rate available on the digital network.

The frequency band occupied by the 900-channel hypergroup signal is 312–4028kHz, which is moved to the band 60–3776kHz by the frequency translation stage in the encoder. The chosen sampling frequency is 7608kHz, giving a half sampling frequency bandwidth of 3804kHz and an output bit rate of 68 736kbit/s, at the minimum acceptable quantization accuracy of 9 bits/sample.

The output bit rate permits a simple multiplexing of two codec outputs to 140Mbit/s (139 264kbit/s) for transmission over the network. This multiplexing, carried out in a fourth-order digital multiplex equipment which is not part of the codec, is necessary since there are at present no plans for transmission at the 68Mbit/s level over the network. Alternatively the multiplexing may be used to combine the codec output with the output from a 68Mbit/s video codec or a suitable assembly of digitized telephone channels.

Noise performance

The noise introduced into the f.d.m signal path by the codec, due primarily to the quantization process in the analogue-to-digital converter with a small contribution from the purely analogue parts of the codec, is an important aspect of the overall system performance since in use the codec and its digital link should not introduce any more noise than the f.d.m link it replaces. Noise resulting from occasional errors in the received digital signal is likely to be at an insignificant level, making the noise introduced by the codec itself the dominant source.

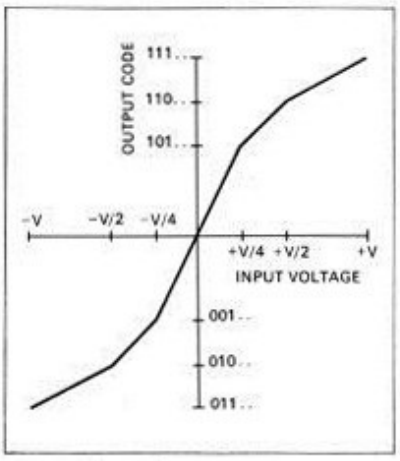

Fig. 3. Non-uniform quantizing law

Figure 2 shows a plot of the theoretical quantizing and peak clipping noise as a function of the system load T_{max} defined as the ratio of a sinusoidal signal just filling the a–d converter to the 0dBm0 test level. The curves shown

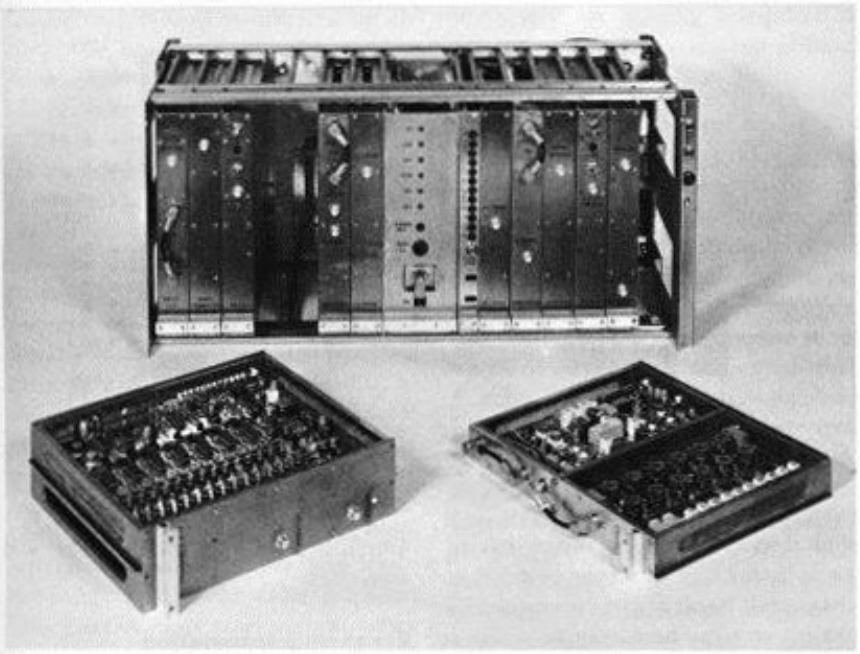

Fig. 4. Prototype equipment with two units removed

are for a fully-loaded hypergroup signal using a quantization accuracy of nine bits/sample. In the case of linear quantization, shown in curve (a), it is seen that the noise at the optimum load level is approximately 400pW0p (pW0p–picowatts psophometrically weighted, referred to a point in the system where the test level is 1mW).

In practice it is possible to use a non-uniform quantization law to effect an improvement in this performance as indicated by curve (b). This is possible since a fully-loaded hypergroup signal approximates to Gaussian noise, enabling the larger amplitude levels, which occur less frequently, to be quantized more coarsely than the lower levels. The quantization law adopted is that shown in figure 3, equivalent to 10-bit linear quantization for levels below quarter full scale, reducing to nine bits between quarter and half full scale, and eight bits above this.

The quantizing noise using this non-uniform law is reduced to just over 200 picowatts at the optimum load level of +27dBm0. In practice it is necessary to add a margin of 2 to 3dB for implementation losses in the a–d and d–a converters and approximately 100 picowatts for noise contributed by the purely analogue stages, to give a value for the total noise contributed by the codec of 500 picowatts (−63dBm0p). At reduced traffic-loading levels the noise performance will improve by up to 2dB due to the non-uniform quantizing, but a more effective improvement can be obtained by use of an automatic gain control to be described later.

Implementation

Figure 4 shows a view of the prototype equipment, constructed in British Telecom TEP-1E equipment practice, modified to accept fully-screened units for the low-level analogue parts of the equipment. The encoder units are situated at the left-hand side of the eight-unit-high shelf assembly, decoder to the

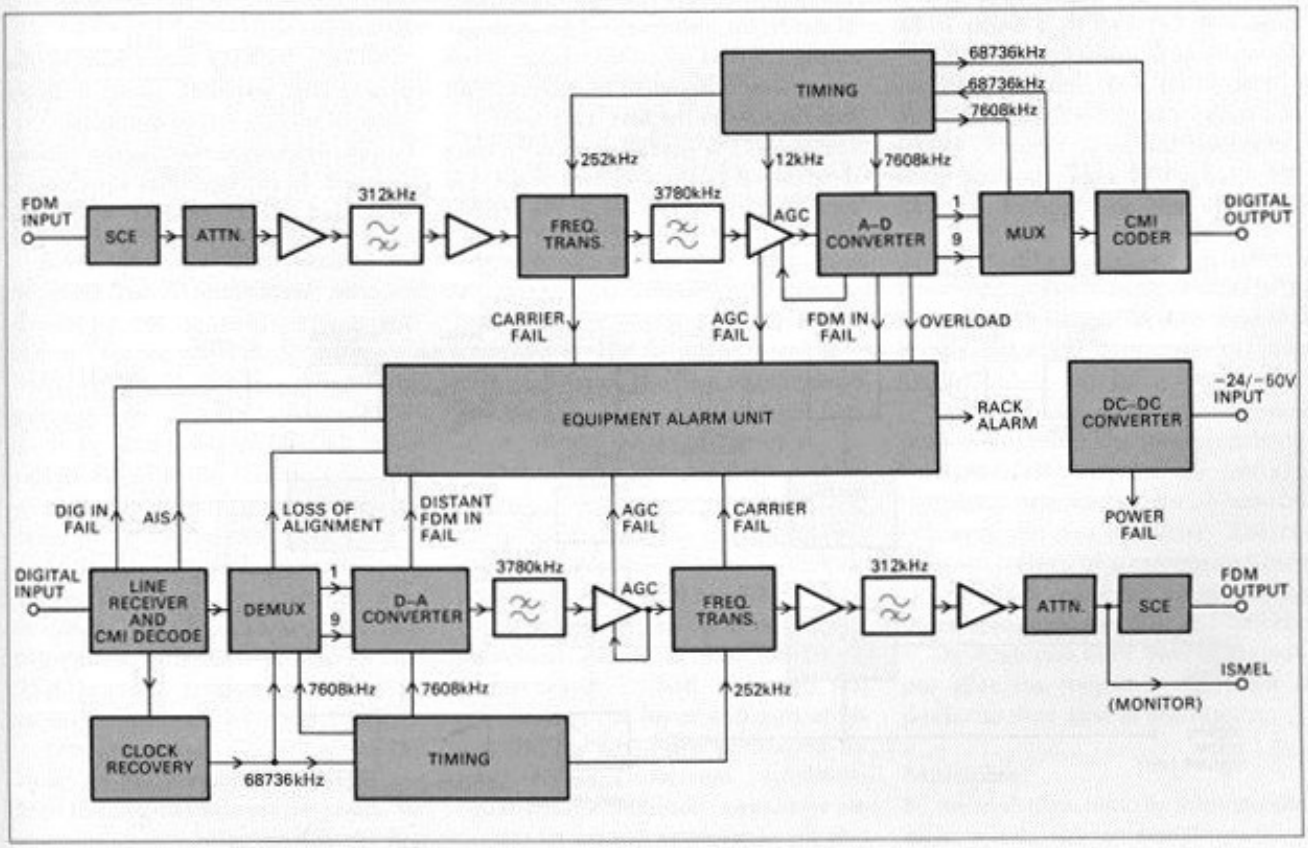

Fig. 5. Detailed block diagram of codec

right, with power supply and equipment alarm unit in the centre. An end-of-shelf alarm unit is located at the far right-hand end of the shelf.

The screened units have been constructed by replacing the conventional plug-in circuit cards with a metal plate on which is fabricated a screened enclosure. Figure 4 shows two units withdrawn with screening covers removed, the analogue-to-digital converter on the left and final output amplifier and station cable equalizer (s.c.e) network to the right. Connection between units is made via individual coaxial connectors with multi-way connectors reserved for the purely digital units, a–d and d–a converters, power supply and alarm units.

Figure 5 shows a detailed block diagram of the equipment, indicating the distribution of timing signals and connections to the equipment alarm unit. A brief discussion follows of the implementation of the principal parts shown in the diagram.

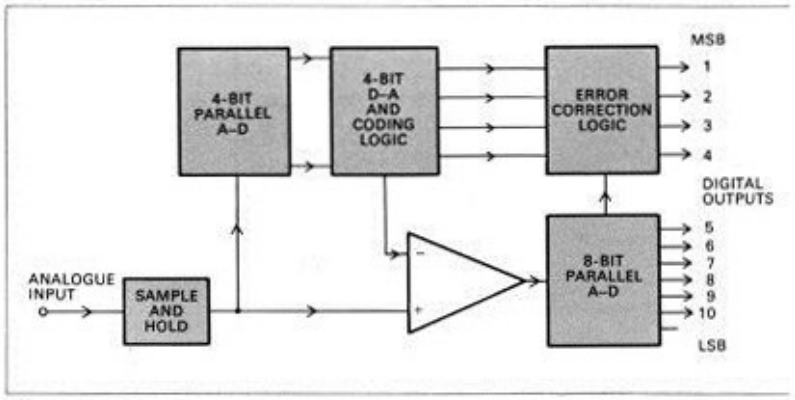

Fig. 6. Ten bit analogue to digital converter

Analogue-to-digital converter

The quantization process is carried out by means of a 10-bit linear a–d converter followed by a digital compression stage to obtain the 9-bit non-uniform law of figure 3. At the decoder a complementary digital expansion is employed, followed by a linear 10-bit digital-to-analogue conversion.

The 10-bit a–d converter uses the two-stage parallel-serial-parallel arrangement shown in figure 6. In the first stage a 4-bit approximation of the sample is made and applied to a 4-bit digital-to-analogue converter having an accuracy of output level better than the overall 10-bit accuracy required for the converter. The output from this is subtracted from the input sample to obtain a residue which is subsequently amplified and passed to the second stage to complete the required overall degree of resolution.

The a–d converter used in the second stage is an integrated-circuit 8-bit all-parallel device designed for TV video encoding, used at only 7-bit resolution to ensure better than ½ least significant bit (l.s.b) accuracy. The most significant bit from this converter is added to the four bits generated by the first stage to obtain the four most significant bits of the 10-bit conversion. This arrangement, referred to as over-range error correction, is designed to correct small inaccuracies in the first stage 4-bit a–d converter. The overall accuracy is then determined by the accuracy of the d–a converter in the first stage, the residue amplifier and the second-stage a–d converter.

Frequency translation

The frequency translation stage in the encoder shifts the frequency of the 15-supergroup assembly down by 252kHz so that prior to analogue-to-digital conversion the signal occupies the band 60–3776kHz. In the decoder the signal frequency is raised by the same amount.

To ensure that there is no net frequency error in passing through a codec the 252kHz reference used in the translators is locked to the system frame rate. Thus exactly complementary shifts are used in the encoder and distant decoder.

Since a 252kHz translation of the hypergroup assembly using a single stage of mixing would result in overlapping sidebands, two stages of mixing are used. In the first stage the signal is translated up to 10MHz where the

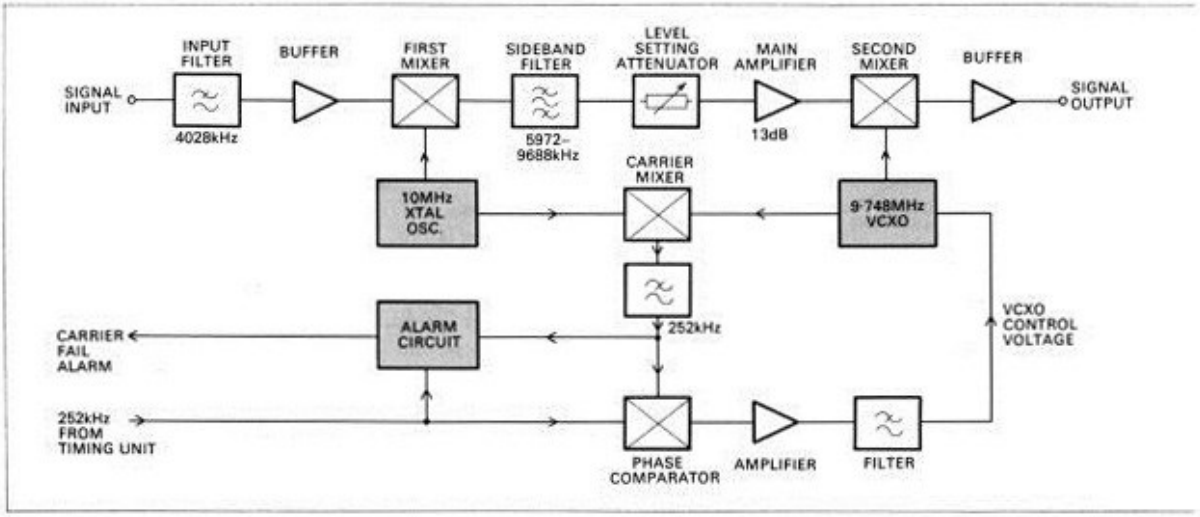

Fig. 7. Frequency translator

unwanted sideband is removed by filtering. In the second stage the signal is down-converted using a second carrier which differs from the first by 252kHz.

The down-conversion stage used in the encoder is shown schematically in figure 7. The low-pass input filter begins to roll-off after 4028kHz and protects the first-stage mixer from image frequencies and out-of-band components which could break through directly to the mixer output. The signal mixers are of the monolithic quad transistor type and receive a balanced drive via transformers.

After the first stage of mixing the required lower sideband occupies the band 5972kHz–9688kHz and the separation between upper and lower sidebands is 624kHz. The sideband filter has five finite poles and exhibits a particularly steep high-frequency roll-off to achieve the required 80dB rejection of the unwanted sideband. Below 5972kHz the filter characteristic rolls off more gently in order to suppress unwanted signal breakthrough to the second mixer.

The second mixer stage uses a carrier frequency of 9·748MHz derived from a voltage-controlled crystal oscillator (v.c.x.o) locked to a frequency 252kHz below the 10MHz carrier. The upper sideband from the second mixer is removed, along with any other out-of-band component, by the low-pass filtering provided prior to analogue-to-digital conversion. Any residual carrier leak which appears in-band at 252kHz will be translated to 504kHz by the receive translator. This lies between channels at the boundary between groups 4 and 5 in supergroup No.2.

Each translator also contains the required carrier-generating circuitry driven by self-contained crystal oscillators. The two carriers are applied via buffer circuits to an active mixer which extracts the 252kHz difference frequency. After low-pass filtering this is compared with the reference 252kHz generated in the timing unit. The phase comparator output, after amplification and filtering, is used to control the v.c.x.o frequency. In addition to a simple RC loop filter an active carrier-suppression filter is used to remove the 252kHz carrier frequency and its harmonics from the v.c.x.o control voltage.

The up-converter used in the decoder employs a similar scheme but here the two carriers are reversed, the lower frequency being used in the first stage and the higher in the second. In addition, extra filtering is required at the output to remove the out-of-band components.

Automatic gain control

The plot of theoretical peak clipping and quantizing noise shown in figure 2 assumes a fully-loaded hypergroup signal. In practice the loading level will vary depending upon traffic conditions, making an automatic gain control desirable if the a–d converter is to be operated at the optimum signal level. For this reason an a.g.c stage has been provided before the a–d converter, controlled by a digital detection of signal level from the a–d. At the decoder, the correct signal level through the codec is restored by a second a.g.c stage after the d–a converter which is controlled by detection of a low-level (−20dBm0) pilot tone injected out of band (12kHz) at the encoder. At low traffic-loading levels an improvement in the quantization noise performance of up to 8dB can be obtained. Any further improvement is restricted by residual noise in the analogue circuits outside the a.g.c loop and by the fact that as the traffic loading falls the signal departs from its approximation to Gaussian noise. A range of control is also provided in the opposite direction to accommodate up to 4dB increase in signal level above the nominal fully-loaded level, with a corresponding increase in quantizing noise.

Input and output filters

High- and low-pass filters are used at the input to the codec to protect against out-of-band input signals, especially signals which could be translated into band by the sampling process. Similar filters are also used at the codec output to prevent out-of-band components from being transmitted to following equipments. The frequency translators have their own filtering requirements and the extra filters required are contained within the translator units.

The overall pass-band flatness of the codec is required to be better than ±0·5dB; in addition the maximum gain change allowed over a 240kHz supergroup is less than 0·3dB. This requires that the pass-band response of individual analogue units should be within about ±0·1dB. To meet this specification the input and output filters and the frequency translation filters require associated amplitude equalizers. Amplitude equalizers to correct for station cable losses are also provided at the f.d.m input and output ports. Each of these station cable equalizers can correct for up to 4dB cable loss at 4028kHz.

The main signal filters and amplitude equalizers have been designed and analysed using a suite of computer programs developed for filters with an equi-rippled pass-band and arbitrarily specified stop-band.

The initial design of the amplitude equalizers was based on the Q-modelled response of the filters and in most cases computer optimization techniques have also been used.

The input low-pass filter requires a sharp roll-off to prevent out-of-band components above the half sampling rate frequency of 3804kHz being reflected into the signal pass-band by the sampling process (aliasing). To accommodate a 14-supergroup assembly, without frequency translators, the pass-band extends to 3780kHz. A 5-pole equi-rippled Cauer-Darlington response filter is used in this position. The stop-band response is at least 10dB down at 52kHz above the band edge and is always better than 40dB down above 4404kHz. After amplitude equalization the pass-band is flat to within ±0·15dB.

The requirements for the input high-pass filter are less stringent and a 3-pole filter is used. The stop-band performance is better than 30dB down below 264kHz and better than 40dB down below 12kHz.

The output low-pass filter is also a 5-pole design and must prevent out-of-band components interfering with subsequent equipment. Again, to accommodate a 14-supergroup assembly, 312–3780kHz, the pass-band edge is 3780kHz. The stop-band rejection is better than 60dB from 4028kHz to 4404kHz. Above 4404kHz the rejection reduces but always remains better than 40dB.

The amplitude equalizer for the output low-pass filter also incorporates the correction required for the $(\sin x)/x$ frequency response of the re-sampler following the d–a converter. The re-sampler consists of a sample-and-hold circuit which requires a compensating lift of approximately 4dB at 3780kHz.

The high-pass filter used at the output after the frequency translator is similar to that used at the input.

Multiplex

In the multiplex unit the 9-bit parallel data words, at a sample rate of 7608kHz from the a–d converter, are

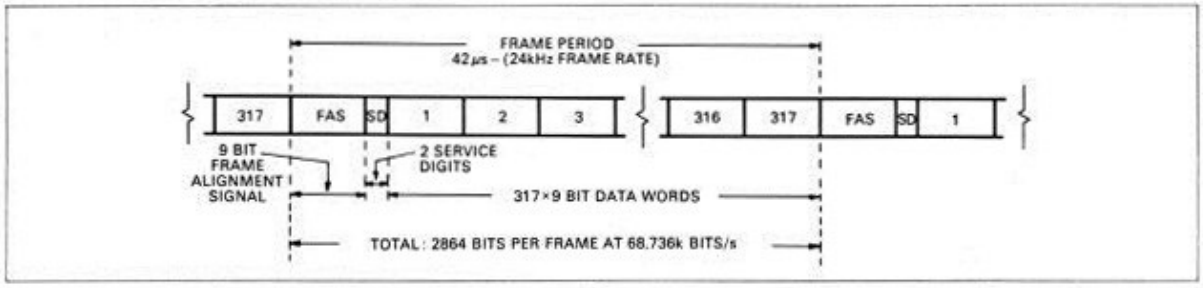

Fig. 8. Frame structure

multiplexed with a resident 9-bit frame alignment signal (f.a.s) and two service digits (s.d), serialized and encoded (coded mark inversion) into a data stream at 68 736kbit/s. As shown in figure 8, a frame contains 317 9-bit data words and with the f.a.s codeword and service digits totals 2864 bits, giving a frame repetition rate of 24kHz. The service digits are used for system equipment annunciation.

To enable the f.a.s and s.d to be inserted at the frame boundary, without temporarily losing data from the continuous input flow, the 9-bit data words are written alternately into two parallel-input/parallel-output (p.i.p.o) buffer stores at a steady 3804kHz (i.e half the a–d sampling rate). Effectively, the data words now exist for twice as long, permitting the store outputs to be sampled alternately with a pause once per frame for interleaving the 11 bits of frame signalling. Each parallel word is loaded sequentially into the transmit shift register that, driven by a continuous master clock, produces a serial stream for c.m.i encoding (figure 9) and subsequent digital output to line at 1 volt peak-to-peak a.c coupled.

Demultiplex

The c.m.i-encoded digital stream is received from line by the demultiplex unit where it is equalized and decoded to provide a serial non-return-to-zero (n.r.z) signal and recovered clock. Detection of the f.a.s in the signal stream synchronizes the demultiplex process: the nine bits of each data word are presented in parallel at 7608kHz to the d–a converter and the two service digits are retained, updated and passed to the alarm unit once per 24kHz frame. While the regular observation of f.a.s indicates demultiplex locked, any incorrect f.a.s is monitored and if four consecutive incorrect f.a.s are received a loss of alignment alarm (l.o.a) is raised and frame search initiated; alignment is regained when three successive f.a.s are correctly detected.

The line receiver provides passive equalization for up to 17dB cable loss (at half bit rate) and raises a digital input failure alarm (dig.in. fail) if the signal drops a further 6dB. Data and clock are recovered from the c.m.i stream by using a driven short-circuited coaxial delay line to provide a half c.m.i symbol period delay. The difference between this and the present input gives a three-level waveform that if sampled in the latter half of each symbol period represents data, while the lower level gives clock information that resides accurately in the negative transitions of the c.m.i waveform.

Provision is made for flagging receipt of an alarm indication signal (a.i.s) which consists of a sequence of all ones instead of true data.

When frame timing has been synchronized, the nine bits of each data word are transferred from a serial receive shift register, alternately into two p.i.p.o buffer stores. Transfer is interrupted at the frame boundary to acknowledge that f.a.s and s.d are not true data. The 9-bit parallel data words are presented to the d–a converter at 7608kHz by reading each buffer store alternately.

Timing

Timing waveforms required by the multiplex and demultiplex processes are generated by their respective timing units; these also provide 7608kHz sample and re-sample clocks and 252kHz for the frequency translators (locked to half-frame rate). The transmit timing also originates a 12kHz a.g.c pilot tone. The basic frame counter comprises a programmable counter dividing by 9 or 11 as required, working at 68 736kHz, followed by a divide-by-318 synchronous binary counter; in general terms this counter provides, for the multiplex and demultiplex, the regular waveforms that require a pause at each frame boundary. The steady 7608kHz sample and resample clocks, and the 3804kHz read-and-write timing originate from 15 216kHz voltage-controlled crystal oscillators by division; these oscillators are phase locked in a narrow-band loop to the mean timing of the frame counter. At the demultiplex this narrow-band loop effectively prevents jitter from the recovered clock affecting the resample timing.

Alarm unit

An equipment alarm unit is incorporated to provide the alarm conditions indicated in figure 5, together with a detection of a high receive error rate at the decoder and generation and detection of a distant alarm condition. These alarm conditions are extended, together with a power-fail condition, to the rack alarm system via the end-of-shelf alarm unit. A separate lamp is provided on the front of the equipment alarm unit card for each of the twelve alarm conditions, together with a common auto reset/lamp lock switch. A separate alarm (red) and receiving attention (green) lamp is provided on the

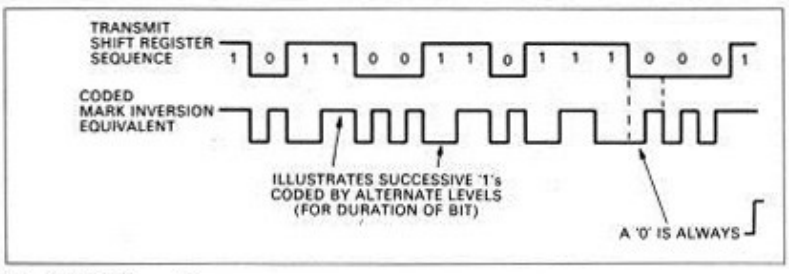

Fig. 9. C.M.I encoding

end-of-shelf alarm unit together with a receiving-attention key.

Power supply

A d.c–d.c converter provides regulated supplies for the equipment at +15V, −15V, +5V and −5·2V from −24 or −50V station battery supplies. A partially-regulated −9V supply is provided for use in the a–d converter. Switched-mode regulation using pulse-duration modulation is employed, together with self-restoring over-voltage and over-current protection.

Conclusion

The article has described the design of an f.d.m hypergroup codec, which will enable a 900-channel hypergroup signal to be carried over a 140Mbit/s digital transmission system via a 68Mbit/s input of a fourth-order digital multiplex equipment. The codec offers a relatively simple and efficient means of carrying f.d.m traffic over a digital link, to permit flexibility to be maintained within the trunk telephone network during the transition to a purely digital transmission system.

Acknowledgement

The authors wish to acknowledge the contribution made by other team members to the design of the codec, including the filter design work carried out by Theoretical Support Services at Marconi Research Laboratories. Acknowledgement is also made to British Telecom for permission to publish this article.

Reference

1. D. Corlett: 'A supergroup codec', *Communication & Broadcasting*, (this issue).

RÉSUMÉ

A l'heure actuelle, le réseau téléphonique interurbain du Royaume-Uni fait largement appel à du matériel analogique à multiplex à division de fréquence (f.d.m) qui fonctionne par l'intermédiaire de câbles à paires coaxiales et de faisceaux hertziens. Alors que l'objectif final est de remplacer ceci par un système numérique, l'on s'attend à ce que la transition s'étende sur plusieurs années.

Dans la période intérimaire, il s'agira de trouver un moyen relativement simple et efficace permettant d'acheminer les signaux du matériel f.d.m existant sur une liaison numérique.

Le présent article décrit un équipement qui a été conçu pour acheminer un signal d'hypergroupe f.d.m à 900 voies sur une liaison numérique de 140Mbit/s. L'article étudie le choix des paramètres du système, les performances de niveau du bruit et la mise en oeuvre.

ZUSAMMENFASSUNG

Das Fernsprechnetz in Großbritannien stürzt sich zur Zeit vornehmlich auf analoge Frequenzmultiplex-Ausrüstung (f.d.m), die über Koaxialkabel- und Rundfunk-Relaisysteme arbeitet. Obgleich es letztendlich das Ziel ist, dies durch ein digitales System zu ersetzen, wird sich der komplette Übergang wahrscheinlich noch über einige Jahre hinauszögern.

In der Übergangsperiode besteht also Bedarf an einer relativ einfachen und wirksamen Methode der Übertragung von Signalen von bestehender f.d.m-Ausrüstung über eine Digitalverbindung.

Dieser Aufsatz beschreibt eine Ausrüstung, die dazu gedacht ist, ein f.d.m-Hypergruppen-Signal mit 900 Kanälen über eine Digitalverbindung mit 140Mbit/s zu übertragen. Es wird auf die Wahl von System-Parametern, Geräuschleistung und Durchführung eingegangen.

RESUMEN

La red telefónica interurbana del Reino Unido confía actualmente de manera considerable en el equipo analógico f.d.m (frequency division multiplex) que opera sobre sistemas de cables coaxiales y radio relé. Mientras el fin eventual es reemplazar esto con un sistema digital, no es probable que la transición se complete hasta que pasen varios años.

Entretanto, existe la necesidad de un medio relativamente sencillo y eficiente de transportar señales desde equipos f.d.m existentes sobre un enlace digital.

Este artículo describe un equipo destinado a transportar una señal del hipergrupo f.d.m de 900 canales sobre un enlace digital de 140Mbit/s. Se de consideración a la selección de parámetros del sistema, ruido, funcionamiento e instrumentación.