Second generation 30-Channel PCM Multiplex

W. H. F. Green, B.Sc., C.Eng., M.I.E.E.

Summary The equipment to be described is a second generation 30-Channel PCM Multiplex incorporating novel features in both its mechanical construction and electrical design. A general discussion of the equipment design philosopy is included from which an optimum system is deduced. Details are given of individual unit functions and of the circuit techniques employed. The adaptability of a basic set of cards to a variety of configurations is emphasised.

W. H. F. Green
Mr. Green joined the Baddow Research Laboratories of the Company in 1958 and worked on a wide variety of communications projects. In 1967 he joined the development team working on 24-Channel PCM and was responsible for power supply design. Subsequently he was engaged on the design of digital switching systems and was made a Section Leader in 1972. He was responsible for the development of the 30-Channel PCM Multiplex equipment currently in production, and a wide range of ancillary items. Recent projects include the second generation PCM development described in the paper.

Introduction

The first generation 30-channel PCM equipment has been described previously in this journal[1] and familiarity with that paper has been assumed in the following. This original equipment was designed for the British Post Office in Type 62 Equipment Practice and as such has a limited appeal to other customers. A joint Industry/Post Office venture in construction practice design has resulted in a new format, Tep-1(E)* and second generation 30-channel PCM has been chosen as the vehicle for its introduction. The performance specification for the new design is similar to that in prodaction, being based on CCITT recommendations but the opportunity has been taken of updating circuit designs to take full advantage of modern technology. This results in a cost effective design which meets the exacting standards of the British Post Office and is also attractive in the export market.

In the following, brief descriptions are given of the construction practice together with the considerations which led to the adoption of this particular design. Details of the resulting cards are given and the overall equipment packaging is discussed.

Construction practice

A survey of existing international racking practice reveals that a combination of 600mm width and 260mm depth is fairly common. Tep-1(E) adopts these external dimensions and fits within them a variety of shelf sizes and groupings. Cabling to the equipment is by means of ducts at each side of the rack and front access only is needed, allowing racks to be mounted back to back. Covers give the equipment a completely clean external appearance.

Cards are generally available in two sizes, 100mm x 196mm and 220mm x 196mm. Two-part connectors are employed between cards and back plane, the latter being either printed wiring, wire-wrapped or a combination of both. Up to 192 connections may be made to the larger card via two such connectors, or other combinations including coaxial and high current may be employed. External connections are made via similar connectors.

Design considerations

The experience gained with the present 30-Channel PCM design enabled an estimate to be made of the space required for the Speech Multiplex, Similar considerations for the signalling area resulted in the conclusion that the complete equipment would occupy a three shelf package, with approximately one half of one shelf free for, as yet, unspecified purposes.

The major decision areas in an analysis of cost and performance trade-offs are the channel filtering techniques and codec philosophy. Considering the former, the CCITT recommendations for time slot access imply that transmit and receive channel circuits should be on the same card and a loading of six channels per card is convenient, resulting in five identical cards per multiplex. There is a choice available between passive component low pass filters and hybrid active filters. The latter are available commercially but have

*Tep and Tep-1 are Post Office registered trade marks.

been rejected in favour of passive filters on the basis of cost. The passive filters have been optimized to reduce component count. Whilst this is the economic solution today it is certain that in the future integrated circuit filters will take their place.

Channel inputs and outputs are made via transformers and it is in this area that considerable economy may be achieved. In the traditional division between signalling and multiplexing previously adopted, two to four wire conversion takes place in hybrid transformers situated on the signalling card. Since these have to carry line current they are necessarily bulky and presented a major problem to the signalling card designers in terms of size. Better transformer utilization is obtained if a simple isolating transformer is used on the signalling card and the transformer pair on the channel card made capable of use as a hybrid. This allows the channel card to be used in either two wire (no d.c.) or four wire modes, by insertion or removal of link plugs. Using this system, overall economies are obtained in both the British Post Office and export systems.

In considering the design of the codec (encoder and decoder), the fundamental choice is between 30 single-channel codecs and some form of common codec. Single channel codecs are not developed specifically for 30-Channel PCM multiplexes because the channel end demand is insufficient. If they ever become a design choice it will be as the result of usage in other equipment bringing the price down to a point where they cannot be ignored. Until then a common channel codec represents the optimum solution.

There are available in integrated form, both digital to analogue converters (DACs) and companding digital to analogue converters (COMDACs). Either of these items, used in conjunction with a successive approximation register (SAR) and a comparator greatly reduce the component count of an encoder. The COMDACs are too slow to use singly but may be used to encode groups of six channels if sample and hold circuits are employed. This possibility was examined thoroughly but was not cost effective. The optimum solution appeared to be the traditional encoder implemented with as high a degree of integration as possible. There is a choice between a DAC together with discrete companding logic or multiple COMDACs. The former solution was chosen on the basis of cost effectiveness since by coding at 3MHz it is possible to eliminate the sample and hold circuit without a significant degradation in performance. This would not be true if applied to the slower COMDACs.

The decoder represents a simpler problem in that a single COMDAC is suitable for the task and represents the most cost effective solution.

Multiplex units

The cards to be described comprise the speech multiplex assembly. Time slot access cards may be fitted instead of the first two channel cards, this being accomplished by means of dual shelf wiring. The complete speech multiplex meets fully all CCITT recommendations.

Channel cards

Each channel card carries six transmit and six receive channel circuits. The utilization of the channel input and output transformers in a hybrid

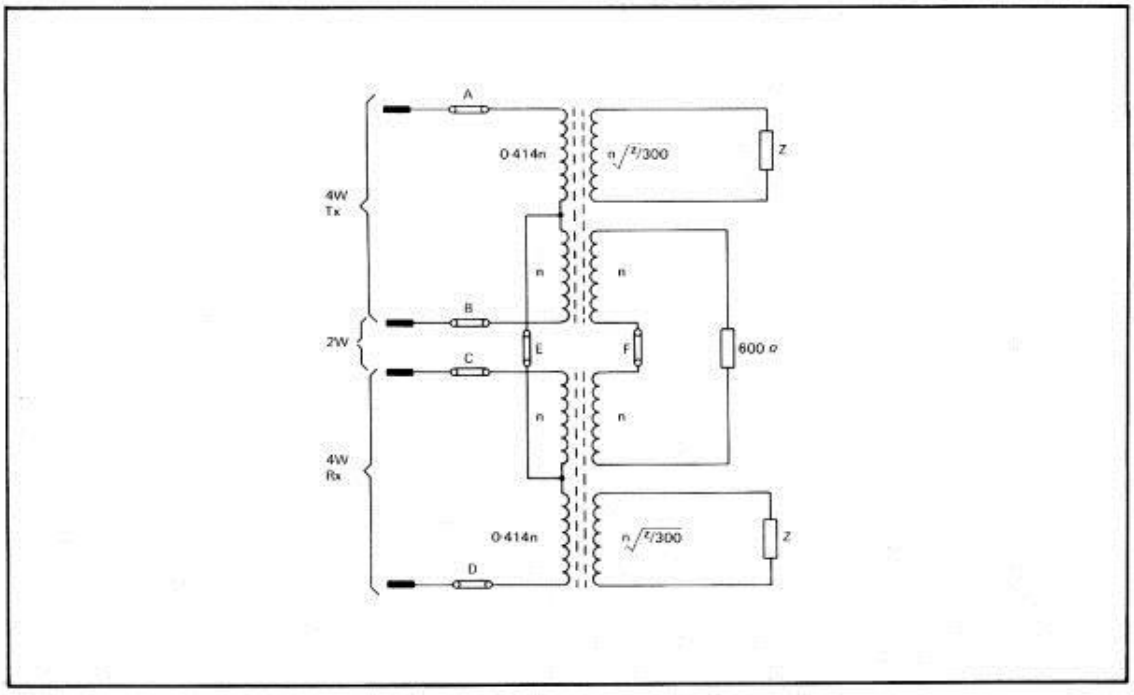


Fig. 1. Hybrid transformer

connection is illustrated in figure 1 where a generalized secondary impedance of Z ohms is assumed. In the particular case of the channel card, the transmit filter input impedance and the receive filter input impedance and the receive filter output impedance are both 1·8 kΩ. With links A, B, C, D, E, F, fitted the card is in the two wire configuration whilst with links E and F removed the four wire configuration is obtained. Links ABCD allow four wire access at the front of the card for test purposes.

The transmit filter has been optimized by use of computer aided design techniques. It is followed by an integrated circuit amplifier whose gain is set by means of a select on test resistor. In the British Post Office system this is the only means of level adjustment and is set during factory test. In order to cater for different transmit levels in export equipment, a stepped attenuator may be fitted in the filter. This is of 1.8 kΩ impedance and has five sections of ½, 1, 2, 4 and 8dB. The attenuator itself is of single in line thick film construction and is linked along its top edge, thereby economising in board area. The signal is a.c. coupled out of the transmit filter in order to eliminate any problems of amplifier offset.

The input to the receive filter originates from a hold capacitor and buffer amplifier in the decoder where the reconstructed p.a.m. sample is held for the whole frame period. This causes the receive frequency response to suffer from aperture distortion of the form of (sin x)/x and compensation for this effect is introduced into the receive filter. Use of sophisticated design techniques enables this correction to be incorporated without the use of any extra components.

An integrated circuit is used to amplify the signal to the correct level, with factory gain adjustment by means of a 'select-on-test' resistor. In addition, the British Post Office require an optional 3dB attenuator which is provided by a further resistor in the amplifier feedback loop. In order to cater for the possible range of signal levels required in export equipment, an attenuator identical to that described in the transmit filter may be fitted in the receive filter.

Time slot access

Twelve channels of the speech multiplex may be utilized for alternative signals. This is achieved by replacing the first one or two channel cards by time slot access cards. The alternative signals may take a number of forms: for example, a number of discrete 64 kbit/s channels, or a number of higher bit rate channels. International agreement will eventually determine the exact format of these signals.

Transmit timing

This card carries all the logical functions associated with the transmit side of the speech multiplex. The system clock is generated by a 12·288 MHz crystal oscillator under varactor control in a phase locked loop. This oscillator may be synchronized to external sources of 2·048 MHz if required by means of optional links on the card. Divider chains produce the 3·072 MHz clock required by the encoder and the 2·048 MHz signal clock. Further division produces clocks at rates down to 4 kHz for use in the codec and within the transmit timing card itself.

Signalling data from the signalling multiplex is clocked into a register at 64kbit/s and clocked out at 2·048 MHz during time slot 16. Framing information and the spare bits are assembled on the card and clocked out during time slot 0.

Data from the time slot access cards (if fitted) is multiplexed with the digital speech signal from the encoder together with the time-slot 0 and time-slot 16 signals and the resulting 2·048 Mbit/s signal is passed through an HDB3 encoding circuit. The signal is converted to ternary form via a line interface circuit.

The card also carries both transmit and receive circuits for a contra directional 64 kbit/s interface, which provides communication between the speech and signalling multiplexes when spatially separated. When the functions are co-sited, these components are not fitted, and communication is provided at TTL levels.

Codec

The Codec is a single card which contains the common analogue to digital encoding, digital to analogue decoding and the encoding, decoding monitoring function of codec test. The analogue multiplexing and demultiplexing of the 30 channels into and out of the encoder and decoder is also carried out on the card. The encoder, a block diagram of which is shown in figure 2, is of the successive approximation type, and encodes in turn each of the 30 input channels and the codec test signal. The 31 inputs to the encoder are multiplexed together in two stages using four 8-input analogue multiplexers followed by a four-input multiplexer which multiplexes together the outputs of the first stage. This two-stage multiplexing arrangement reduces zero offset problems caused by leakage current of the "off" channels. It also results in more time being available to access each channel and reduces the capacitance at the amplifier inputs.

The output of the multiplex forms the input to two buffer amplifiers, the outputs of which provide the low impedance source required by the comparator circuits used. The amplifiers are fast enough for their outputs to settle to the value for a new channel in less than 1·3μs with sufficient accuracy to ensure that the crosstalk between one channel and the next is reduced to less than one quantum step.

The encoding range of the encoder is divided into four parts—positive and negative, with greater or less than 1/16 maximum input. By dividing the input range into greater or less than 1/16 Tmax, corresponding to linear code 128, two 8-bit

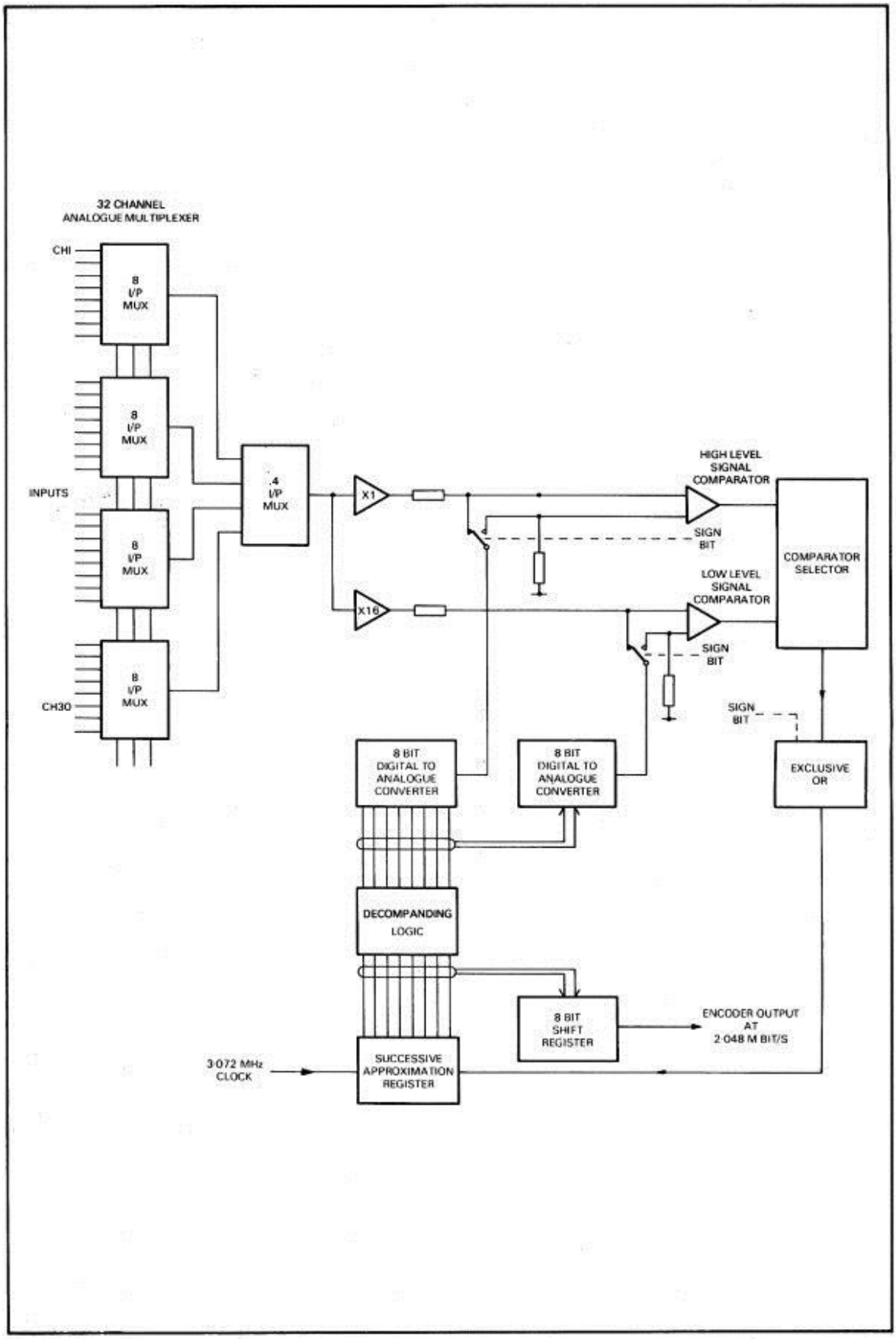


Fig. 2. Codecencoder

accuracy digital-to-analogue converters can be used at the expense of one extra comparator and an extra buffer stage to cover the sign plus 11-bit equivalent dynamic range of the encoder.

The successive approximation register (SAR) is driven by the 8-bit code being generated in 2·60μs. This with the 1·30μs allowed for the input amplifier to settle gives a total of 3·90μs to encode one channel, corresponding to 125μs for one frame. This rate of encoding allows the conventional sample-and-hold circuits to be dispensed with at the cost of an acceptable degradation in performance. The eight outputs of the SAR are registered and shifted out to give a 2·048 Mbit/s output to the Transmit Timing.

The use of a unity gain and x 16 amplifier ensures that the comparators are driven with a suitable level of signal under all input conditions, thereby maintaining their response time. The choice between high or low level comparator is made after the second bit has been decided.

A block diagram of the decoder is shown below in figure 3.

An 8-bit parallel input is applied to the COMDAC either from the Receive Timing or from Codec Test.

The COMDAC produces a current dependant on the code applied such that due allowance is made for the companded nature of the signal and the necessary half step offset. For input codes corresponding to positive signals the current goes into the I+ terminal of the COMDAC and negative signals into the I– terminal. These currents are converted to a bipolar voltage by a fast amplifier.

The low impedance voltage of the amplifier is applied to the input of a 32-way analogue demultiplexer, which takes the form of a two stage sample and hold circuit. As each channel is decoded in turn the corresponding channel capacitor is charged, in less than 7·8μs, to its new value which it then holds for the next 117·2μs. The hold capacitors are each connected to high input impedance buffers. Any droop in the hold mode produces signals at the sampling frequency of 8 kHz and its harmonics which are rejected by the receive filters, as are d.c. offsets by the a.c. coupling employed.

The encoder and decoder functions are checked automatically by a built-in test circuit. This check takes place during time-slot O and causes an alarm to be raised if a fault appears in any of the upper coding segments.

Receive timing

This card performs all the necessary receive timing functions and in addition carries the alarm logic and displays. A line interface circuit converts the incoming line signal from ternary to binary form and provides outputs to the line failure detector, clock recovery circuit and HDB3 decoder. Detection of a line failure results in the main 2.048 MHz clock being derived from the transmit side of the equipment. The HDB3 decoder output feeds the time slot access cards if fitted, the Alarm Indication Signal (AIS) detector and an 8-bit register whose outputs provide data for the frame alignment word detector, the time-slot O spare bits register, the speech word and the time-slot 16 signalling extrac-

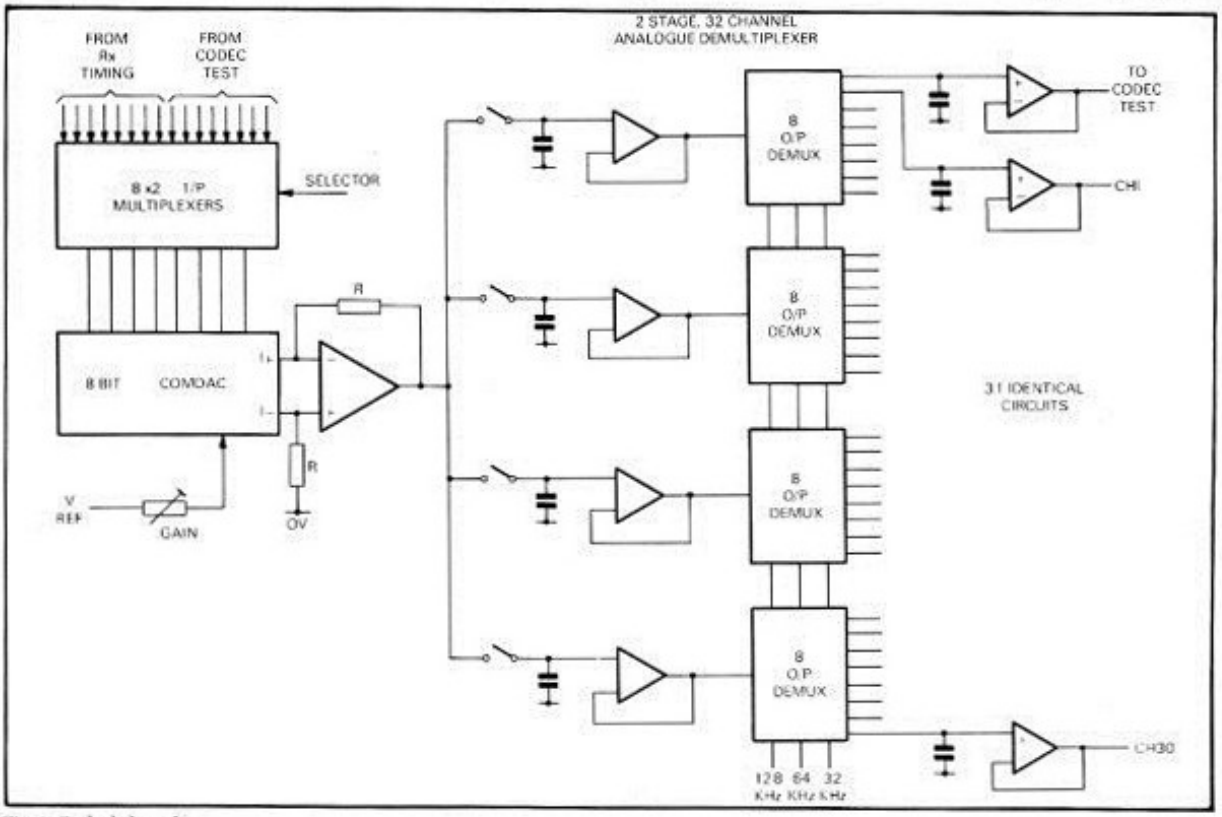
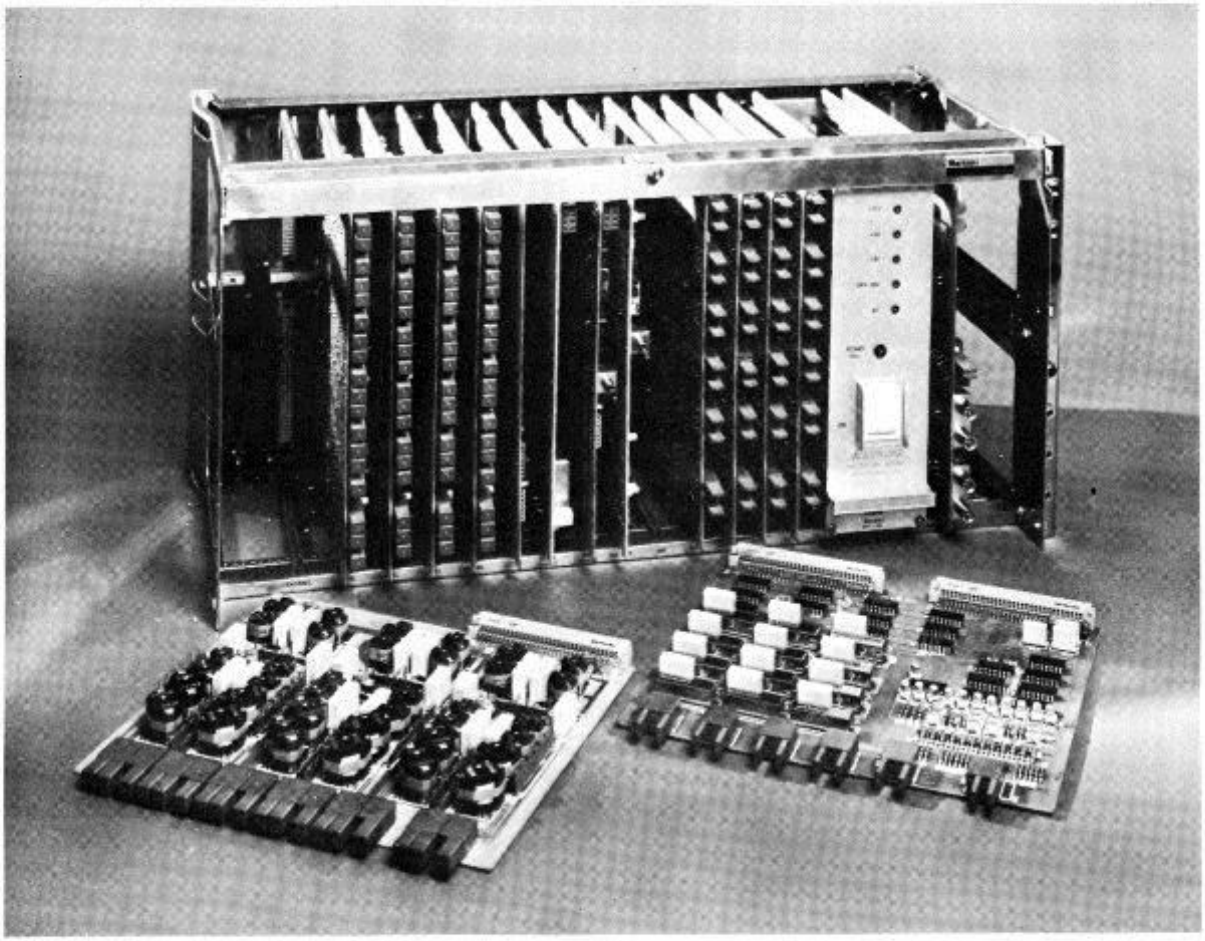


Fig. 3. Coded-decoder



Single shelf multiplex with E & M signalling and line terminal facilities with channel card and signalling card displayed.

tion circuit. The time-slot 16 data is available in forms suitable for both local use and transmission over a 64 kbit/s contra directional interface.

Errors in the received frame alignment word are detected and counted in an error counter. Divider chains provide waveforms from the 2·048 MHz clock down to 4 kHz and further division provides a time base for the error alarm circuit. A strapping link allows the error alarm to be produced by line error rates of either 1 in 10^4 or 1 in 10^3. Loss of frame alignment is assumed when three consecutive frame alignment words have been received, each with one or more errors. This causes the card to enter the frame alignment search mode.

The alarm logic accepts inputs from nine sources, some of them external to the card, and by means of combinational logic produces outputs to perform the required actions. The alarms are displayed along the front edge of the card by means of light emitting diodes, which are provided with a lamp lock/auto reset switch.

Strapping links within the card enable a number of options to be selected, including the designation of alarm conditions as prompt, deferred or in-station. This designation is signalled to the rack alarm unit via suitable interfaces onto a 10-wire alarm bus. Further interfaces allow shelf status indicator lamps to be illuminated. In certain circumstances a service alarm is sent to the signalling multiplex.

Power supply

Two power units have been designed, both of which operate on any input from −20V to −60V and supply ±15V and +5V. They differ in size and output power capability; the larger unit is capable of supplying a standard British Post Office speech and signalling multiplex equipment whilst the smaller supplies either a single shelf export system or under certain circumstances, two speech multiplexes.

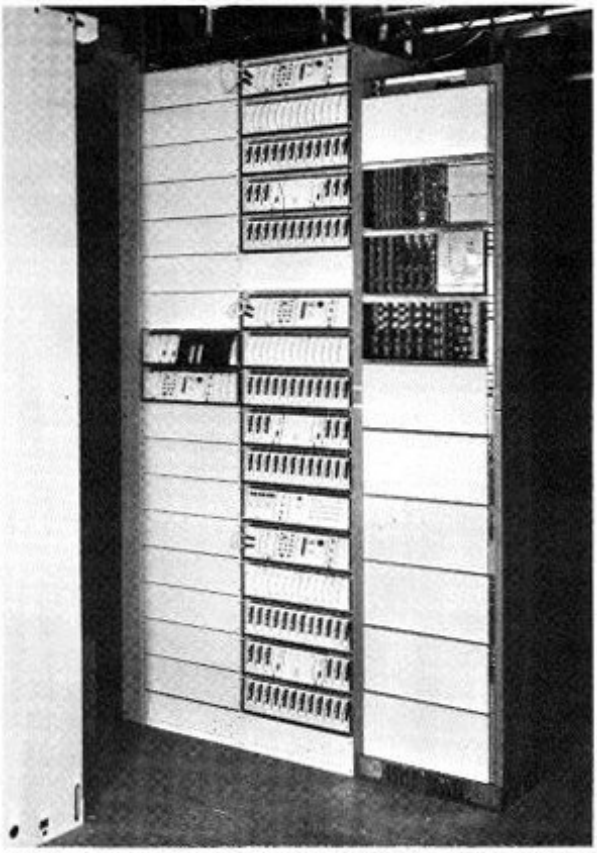
Both units are designed on the same principles, that is, switched-mode operation using pulse duration modulation to achieve output regulation. The units employ wholly electronic self-restoring overvoltage and overcurrent protection. This results in any fault condition appearing as a "low voltage" output, which is the only alarm generated by the power units. The units are designed so that no combination of load, either normal or fault can result in any damage to them or associated equipment. The units are extensively screened in order to reduce the levels of both acoustic and electromagnetic radiation to acceptable limits.

Alarm system

As has already been described, individual alarms are displayed on a number of different cards

2nd generation P.C.M. cards undergoing production testing.

within the multiplex. A major feature of the construction practice is that a completely clean appearance is presented by the use of shelf front covers resulting in the obscuring of these displays. Alarm indications are therefore presented in an area adjoining the cable duct cover at the end of each shelf whose units are capable of generating alarms. In the British Post Office system both an Alarm lamp (red) and a Receiving Attention lamp (green) are employed, and connections are made between each shelf and a Rack Alarm Unit (RAU) via an alarm bus system.



P.C.M. multiplex equipment installed in a telephone exchange with previous generation equipment on left.

Packaging

The speech multiplex equipment described occupies approximately one half of a 240mm high Tep-1(E) shelf. In the British Post Office system the signalling equipment and combined multiplex and signalling power unit occupy two shelves. The complete equipment package therefore consists of three shelves with the spare half-shelf located above the power unit to prevent any excessive local heating. This three shelf structure allows a maximum of three complete equipments to be fitted to a 2·6 metre rack.

The standard export equipment, fitted with dual E and M signalling cards, is accommodated in a single 240mm high shelf. A similar set of multiplex cards is used together with a smaller power unit and the standard signalling multiplex card. In addition, a further card may be fitted which interfaces both the input and the output of the multiplex to the line system. It is believed that this complete 'system in a shelf' will prove attractive to overseas buyers. Other packaging possibilities occur if the signalling facility is required to be remotely sited from the speech multiplex. In all cases, the same cards are used, the difference in requirements being met by a set of appropriately wired back planes.

Conclusion

The equipment described will shortly be undergoing a field trial for the British Post Office. A satisfactory outcome of the trial will provide a firm home market on which to base the expected expansion in overseas sales. The successful accomplishment of the programme has been due to the efforts of the development team involved to whom the author also acknowledges his gratitude for their assistance in the preparation of this paper. Permission from the Post Office to publish this article is acknowledged.

Reference

1. H. Thurgood: "30-Channel PCM" Communication & Broadcasting, Vol. 2, No. 2, (Spring 1976) pp. 37-49.

RESUME

L équipement qui sera décrit est un matériel de multiplexage M.I.C. de deuxiéme génération, á 30 canaux, comportant des innovations de construction mécaniques et électriques. Il est inclu une étude d'ordre general des principes de conception de l' equipement ayant donné lieu à un système optimal. Des détails sont donnés sur les diverses fonctions d'unité et sur les procédés de circuits utilisés: on a mis l'accent sur l'adaptabilité d'un ensemble de cartes ou plaquettes de base à diverses configurations.

ZUSAMMENFASSUNG

Die hier beschriebene Ausrüstung ist eine 30-Kanal-Pulszahl-modulations-Multiplexanlage, deren mechanische Bauweise und elektrischer Entwurf neuartige Merkmale aufweist. Ebenfalls eingeschlossen ist eine allgemeine Diskussion der Designphilosophie, wovon sich ein optimales System ableiten läßt. Einzelheiten der verschiedenen Funktionen der Einheit und der hierbei angewendeten Schaltungstechniken sind angeführt. Die Anpassungsfähigkeit eines Grundkartensatzes an eine Vielzahl von Konfigurationen wird betont.

SUMARIO

El equipo que va a describirse es un Múltiplex de Modulación por Impulsos Codificados de 30 Canales que lleva incorporados nuevos dispositivos tanto en su construcción mecánica como en su diseño eléctrico. Se incluye una discusión general sobre la concepción del diseño del equipo a partir dela cual se deduce un sistema óptimo. Se dan detalles de las funciones de unidades individuales y de las técnicas de circuitos utilizadas. Se da importancia especial a la adaptabilidad de un juego básico de tarjetas para una diversidad de configuraciones.