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A new high-stability Eddystone receiver

Summary

The new Eddystone 1837/1838 series of receivers represent a considerable advance in the design of first-grade h.f communication receivers of moderate cost. It is a development of the 1830 series of receivers the good reputation of which is well established. A particular feature of the new receiver is the unique method used for frequency stabilization which combines the convenience of manual tuning with the facility of locking the frequency in increments of 1Hz, when required; it forms the subject of Patent Application No.21292/76.

The receiver is designed to meet the British Ministry of Posts and Telegraphs specifications MPT 1201, 1216, 1217, 1204 and its performance has been approved by the Ministry as complying fully with these specifications.

Introduction

The Eddystone 1837/1838 series of receivers has been designed to meet the requirements of modern communication systems. The frequency of operation is within the range 100kHz to 31MHz, and is indicated on a digital-type LED display. Figure 1 shows the layout

Figure 1. View of the front panel showing the LED frequency display and layout of the controls

of the operating panel, the yellow 10mm LED display being particularly clear and attractive. Push-button switches, with small LED indicators, are used to control most functions.

A double-superheterodyne system is used, as shown in figure 2, with continuous tuning by manual operation of panel controls. The frequencies of the two local oscillators may be varied independently, by adjustment of the 'main tune' and 'fine tune' controls, the latter having a range of ±10kHz. When the desired signal has been selected, a 'lock' button is depressed, bringing into operation the digital drift-correcting circuits, which are controlled by both local oscillators. The signal will then be held indefinitely with a precision adequate for the satisfactory reception of s.s.b and narrow-shift f.s.k transmissions. This high-stability mode of operation is available for all frequencies above 1.5MHz, and also for those below 840kHz.

The production of a receiver of this performance at a modest price has been made possible by the development of a very simple frequency stabilizer together with the use of techniques, of proven merit, previously developed for the 1830 series of receivers.

The drift correction system

The normal methods of obtaining high-frequency stability in a communications receiver use drift-cancelling techniques (such as are used in the Eddystone 958 receiver), or by the use of a frequency synthesizer. Both of these methods tend to cause the generation of spurious signals within the receiver, either as harmonics of the various oscillator and mixer frequencies, or as noise appearing as sidebands on the output of the local oscillators. Great care is therefore needed in their design and construction, and expensive screening and filtering are necessary. In addition, there are usually difficulties in providing the facility of continuous manual tuning.

The system developed for the 1837/1838 series overcomes many of these problems. The operation is simple, and is illustrated in figure 2, which shows a block diagram of the receiver. With the arrangement of oscillator frequencies used, the frequency f_s of the received signal is related to the frequencies of the first and second local oscillators, f_1 and f_2 respectively, and to the second i.f frequency f_i used by the expression

$$f_s = f_1 - f_2 - f_i$$

Thus, assuming no drift in f_i, f_s will remain constant provided that $(f_1 - f_2)$ remains constant, and f_1 and f_2 need not be separately stabilized.

In the 'free tune' mode, f_1 and f_2 are independently adjustable from the panel controls, and the frequency stabilizer (S in figure 2) is disabled. When satisfactory reception of a desired signal has been achieved, the 'lock' button is depressed: in the ensuing 1-second period, the frequencies f_1 and f_2 are measured, and the difference $(f_1 - f_2)$ stored digitally. Thereafter, these frequencies are measured respectively, and their difference compared with the stored value: the error, if any, is used to control f_2, to bring the frequency difference back to its correct value. How this is done will now be described in more detail.

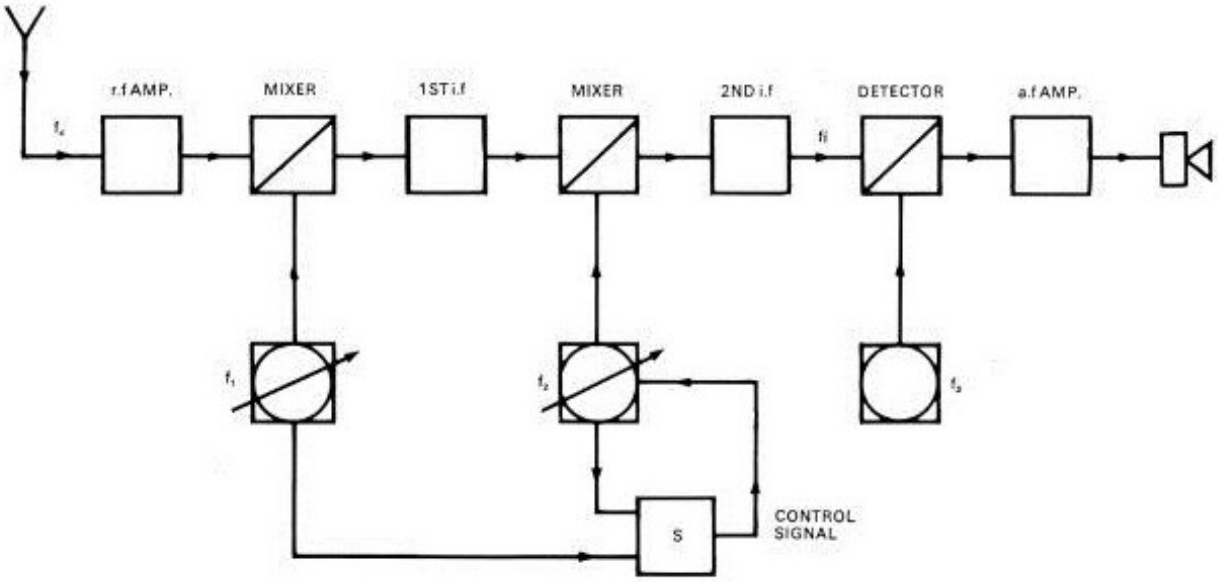

Figure 2. Functional diagram showing the drift-correcting circuit arrangement

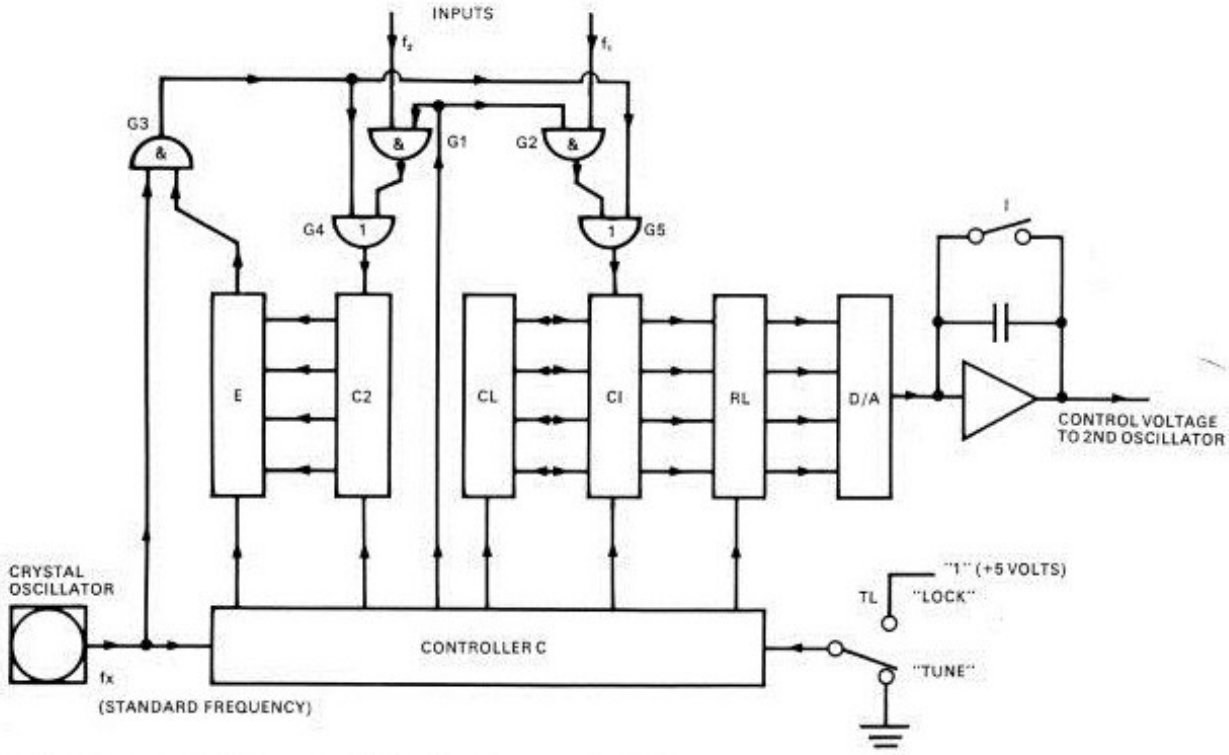

Figure 3. Functional diagram of the digital drift-correcting circuits

Detailed operation of the system

A block diagram illustrating the principles of operation is given in figure 3. In the 'tune' state, all logic elements are reset, the integrator capacitor is short-circuited and the control voltage delivered to the f_2 oscillator is therefore zero. Upon setting the tune/lock switch TL to 'lock', the subsequent action is dictated by the controller C. There are then two phases of operation, the 'initial' count phase, and the 'correction' phase. In the 'initial count' phase, the first operation is the

generation of an accurately timed 1-second pulse within C, which pulse is delivered to the Gates G_1 and G_2, allowing oscillator pulses at frequencies f_1 and f_2 to enter the counters C_1 and C_2 respectively. Upon termination of this pulse, the counts stored in C_1 and C_2 correspond to these frequencies. The next operation is to subtract the count in C_2 from that in C_1 to obtain a total count corresponding to (f_1-f_2). This is accomplished by applying pulses at a frequency f_x (via G_3) to C_1 and C_2 simultaneously, via the OR gates G_4 and G_5, until C_2 is full: this state is sensed by the element E, which then disables gate G_3 and the counting ceases. Thus an extra count, equal to the complement of that originally in C_2, is added to that already in C_1: this operation results in a total count in C_1 corresponding to (f_1-f_2) which is then transferred to the count latch CL by the action of the controller. This completes the 'initial count' phase and occupies a time slightly more than one second.

The operation now enters the 'correction' phase, where it will remain until the receiver is retuned. Here, the controller first transfers the complement of the count stored in CL back to C_1. The count cycle of the 'initial count' phase is then repeated: the 1-second timing is applied to G_1 and G_2, f_1 and f_2 are counted into C_1 and C_2 respectively, and the complement of C_2 added to the count already in C_1. The result is a residual count in C_1 corresponding to the difference Δf between the value of (f_1-f_2) when the count is made, and that value measured in the 'initial count' phase, *i.e* the frequency drift of the receiver in this period. The residual count in C_1 is now transferred to the 'residue latch' RL, which is connected to a D/A converter, and the output current of the latter is applied to the integrator I. The integrator output controls the frequency of the second oscillator, tending to correct the frequency error Δf. This cycle of operations in the 'correction' phase is repeated at approximately 1-second intervals.

It will be noted that, due to the action of the integrator, the control voltage to the second oscillator is applied smoothly, and the resulting absence of sudden transient changes in f_2 ensures that no adverse effect on the receiver performance is caused by the action of the stabilizer.

The frequency drift occurring between successive cycles of correction is normally very small, and the capacity of the counters need not be as great, therefore, as the whole count of f_1 and f_2 during the 1-second timing period. The counters, latches and D/A converter are limited to 8 binary digits, giving an allowable maximum frequency error between cycles of $\pm$127Hz. Experience has shown this to be adequate for the conditions of shock and vibration required by the MPT specifications. The performance under these conditions is greatly helped by the use of a solid-dielectric variable capacitor in the first oscillator.

The total long-period drift correction possible is limited by the maximum output voltage excursion of the integrator, and corresponds to an error of $\pm$10kHz. In the unlikely event (perhaps after a very long period of operation) of the frequency drift exceeding this value, the fact is indicated to the operator by a periodic interruption of the LED display on the control panel.

DIGITAL FREQUENCY DISPLAY

An expression for the frequency f_s to which the receiver is tuned has already been given as $f_1-f_2-f_i$. This frequency is measured using a reversible counter: the value of f_i (100kHz) is first loaded into the counter before counting starts; the frequency f_2 is then counted 'down' for a 200ms timing period followed by a similar period when f_1 is counted 'up'. The result is then transferred to the count latch, which activates the LED display; this consists of six decimal digits, giving an indication of frequency in increments of 100Hz.

The values of timing period and display frequency discrimination have been carefully chosen for greatest convenience of the operator: the displayed numbers readily follow the tuning operation, and are virtually free from the erratic fluctuations often associated with this type of frequency display.

Design feature

The application of the error signal to the second oscillator only is an important feature of the new stabilizer. Attempts have been made before to design stabilizer systems with the error signal applied to the first oscillator, which necessarily covers a wide frequency range. As a result, the sensitivity of control varies greatly over the tuning range, and there are considerable difficulties in achieving an acceptable dynamic performance of the error feedback loop. With the system used in the 1837/1838 series these problems do not arise, as the oscillator to which the control signal is applied operates at a relatively low frequency with only a narrow tuning range. Also, since no control voltage is applied to the first oscillator, the good reciprocal mixing performance associated with the use of a simple high-quality oscillator for this function is preserved.

The performance of the 1837/1838 receiver is at least an order of magnitude better than that required by the MPT 1201 specification, in respect of frequency stability, with variation of ambient temperature and supply voltage. The receiver also easily satisfies the shock and vibration requirements of this specification.

Signal circuits

The design of the signal circuits in the receiver follows established practice, the operations of amplification and mixing being carried out by a carefully chosen range of integrated circuits and discrete devices. The use of a ceramic filter in the second i.f amplifier ensures an excellent s.s.b response characteristic.

Three types of output are provided; a low-level, low-impedance 100kHz output suitable for driving ancillary equipment, and audio outputs for connection to medium and low-impedance loads. A variant of this receiver is available having an f.s.k detector and printer drive output.

Construction

Mechanical rigidity of the receiver is ensured by the use of substantial cast metalwork, which also provides effective screening. The power consumption of the receiver is approximately 50 watts and the power supply unit is sufficiently versatile to accommodate most of the world's supply voltages.

Conclusion

The Eddystone 1837/1838 series of receivers is suitable for most general purpose communication applications, including marine use, where speech, telegraphy or f.s.k teleprinter signals are employed. At moderate cost, the receiver provides the convenience of manual tuning with a high-stability mode of operation, thus ensuring that once the desired signal has been tuned in, the receiver will stay on-tune indefinitely in spite of wide variations in temperature and supply voltage.

A high degree of reliability is an important feature of the design; the receiver has been designed to maintain its performance under severe environmental conditions of climate and location under which it will provide a long and reliable service.